

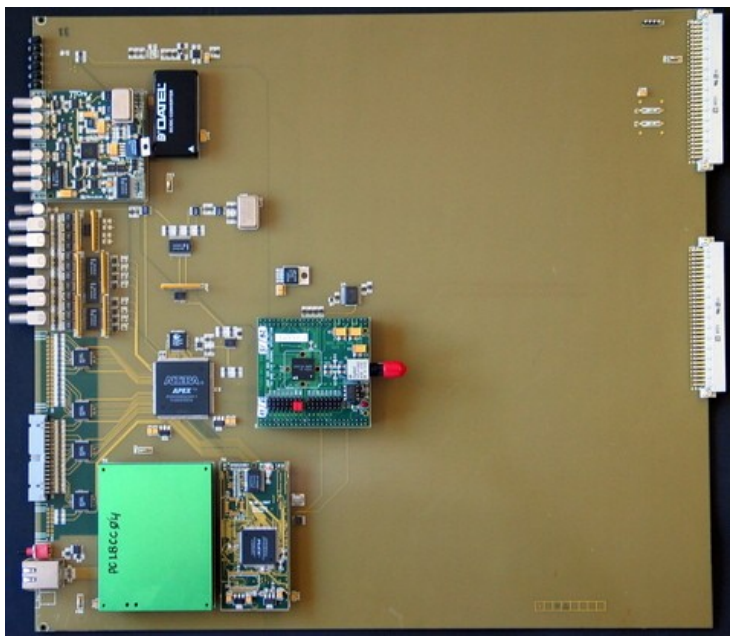
oliscience

open logic interconnects science

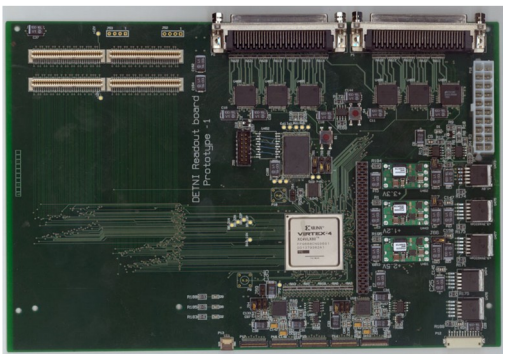
Andrea Borga co-founder and CEO

About me

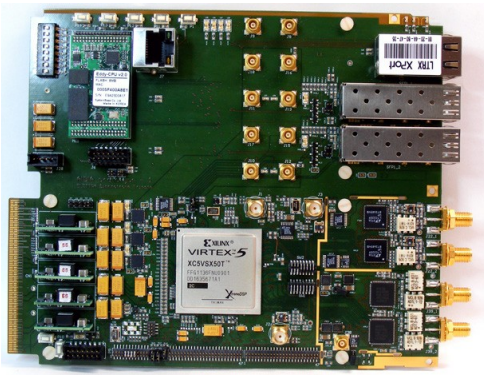
- Digital Designer “FPGA guy” specialized in Data AcQuistion (DAQ)
- I (still) love science!8)



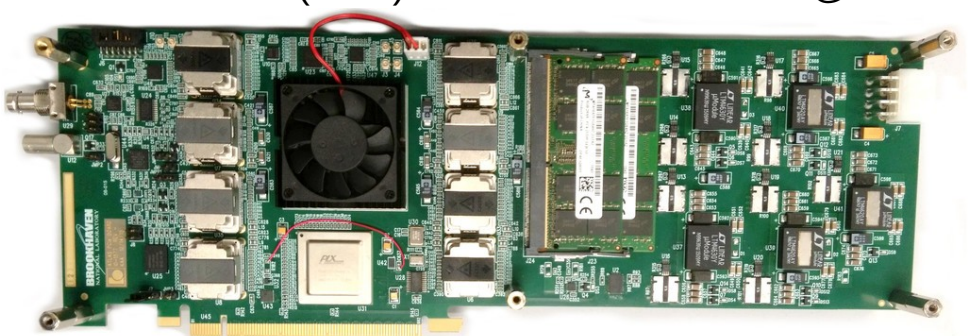
CERN – LHCb (2004)



FZ-Juelich – DETNI (2007)



Elettra – FERMI@Elettra (2011)



Nikhef – ATLAS (2019)

About Oliscience BV

- Originating from the CERN-BIC at Nikhef





- Trained at the Amsterdam Centre for Entrepreneurship (ACE)
- Based at the Amsterdam Science Park

Oliscience management team

- Alberto Alberton: (sales and marketing)
  - → experienced entrepreneur
  - → angel investor in oliscience
- Leo Davoli: (legal and operations)
  - → professional lawyer
  - → angel investor in oliscience
- Andrea Borga: (CEO)
  - → seasoned digital design engineer
  - → passionate technologist
  - → open source enthusiast
  - → the geek!







Oliscience management moments

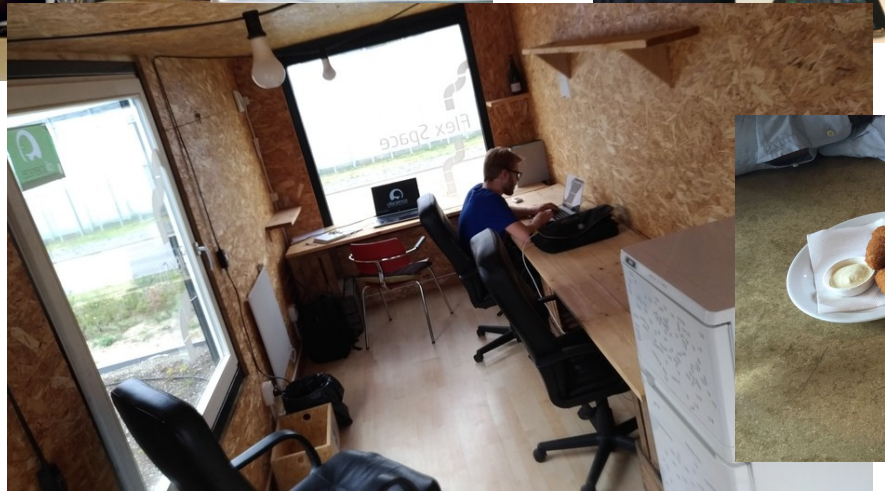










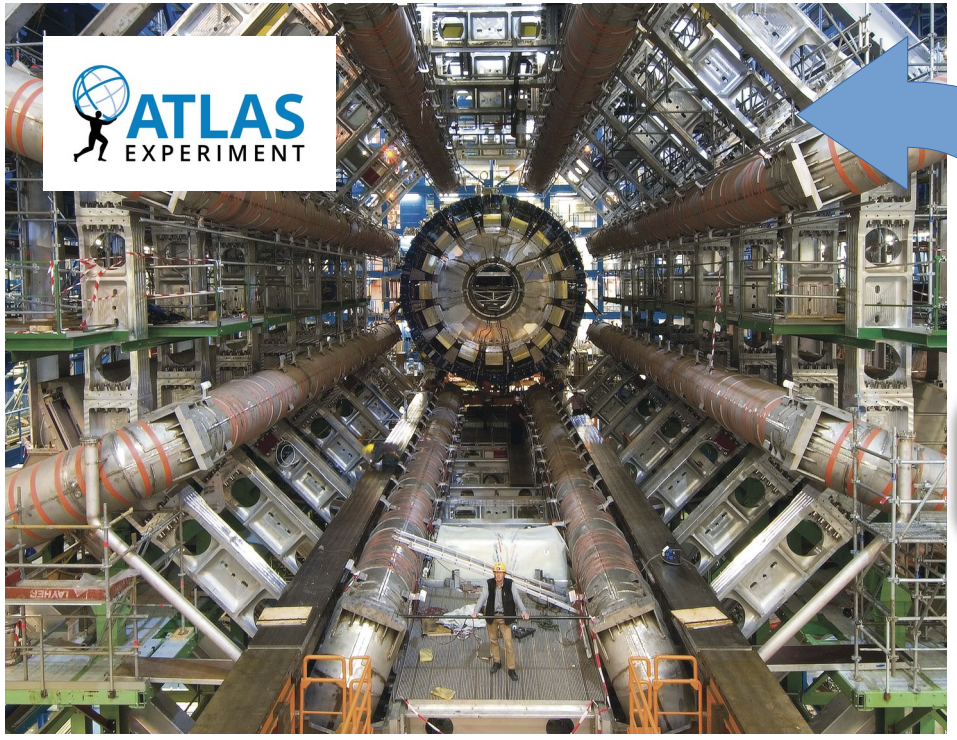




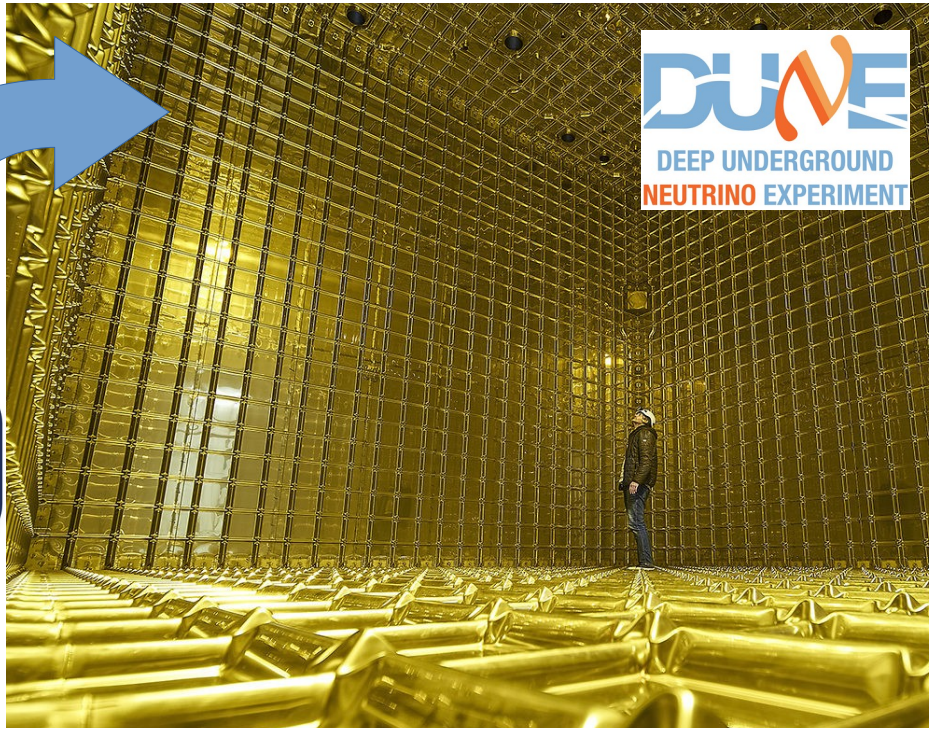
Oliscience in a nutshell

- Core business: FPGA technology
- **Innovating in the field of FPGA**
- Stewarding the OpenCores.org platform
  prominent portal for Open Source IP exchange
  → “we are the GitHub for FPGA”
- Lean Design House providing consultancy

Consultancy customer

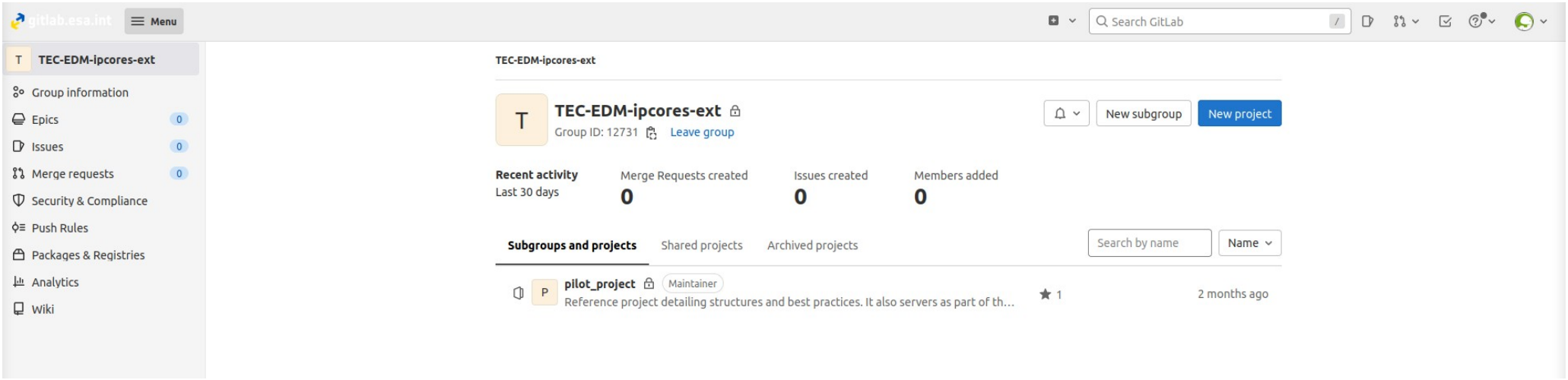






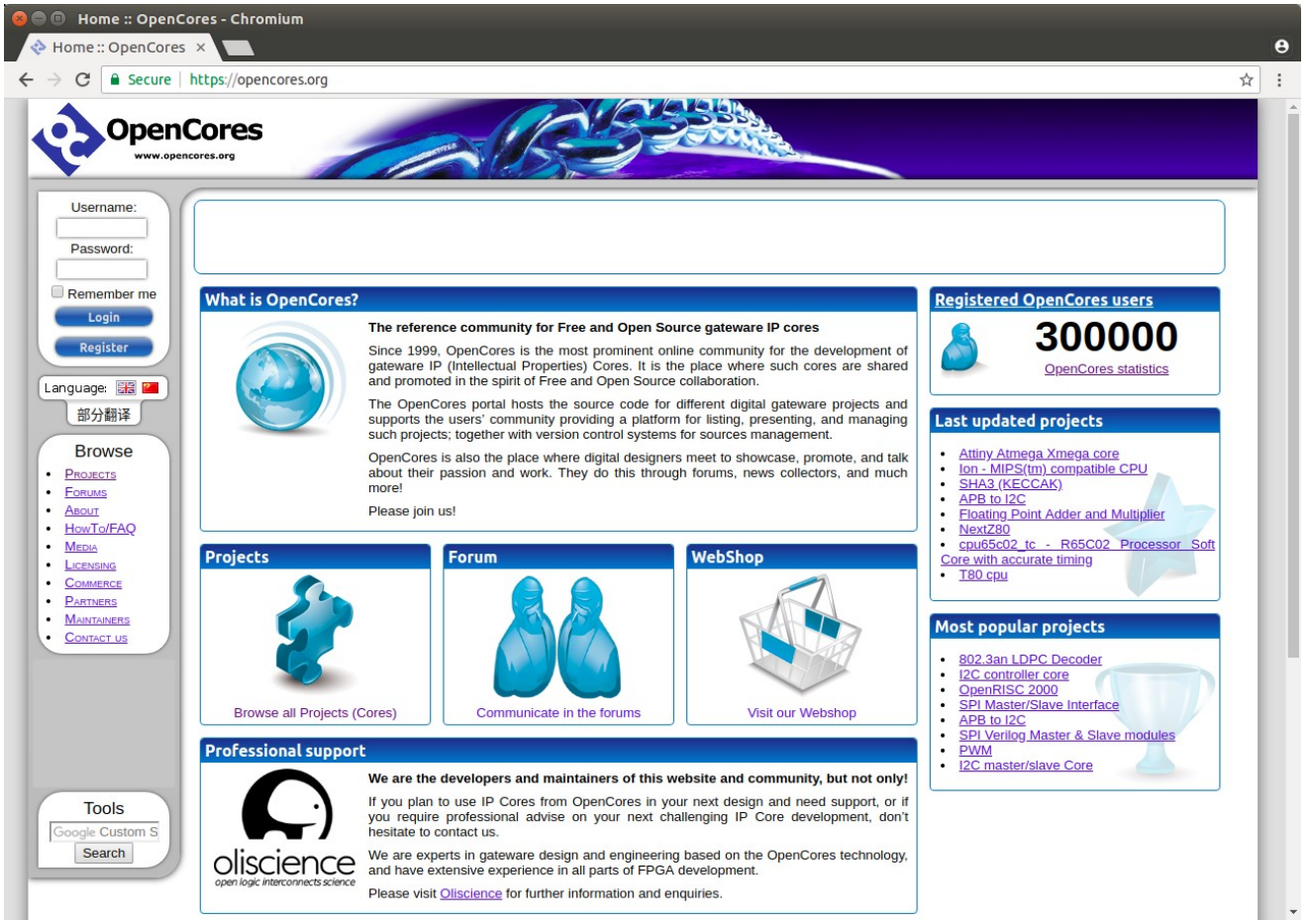
- Open Source facilitates technology transfer

Consultancy customer



- Mentoring distributed collaboration best practices

The “good old” OpenCores.org



OpenCores.org in numbers

- Made in Europe!
- Founded in 1999
- Regularly used by >370.000 professionals
- Generating ~500.000 views per month
- 1267 IP Cores covering a very broad spectrum
- **Acquired by Oliscience in 2017**
- Still strong identity, established trademark, consistent community, very specialized

OpenCores.org purpose

- OpenCores brings together Digital Design Engineers
- **make FPGA and gateware more accessible**
- **push!** ensure that the best IP Cores are used and let them be improved further by community
- **pull!** encourage more people to add IP Cores

Foster Open Source culture



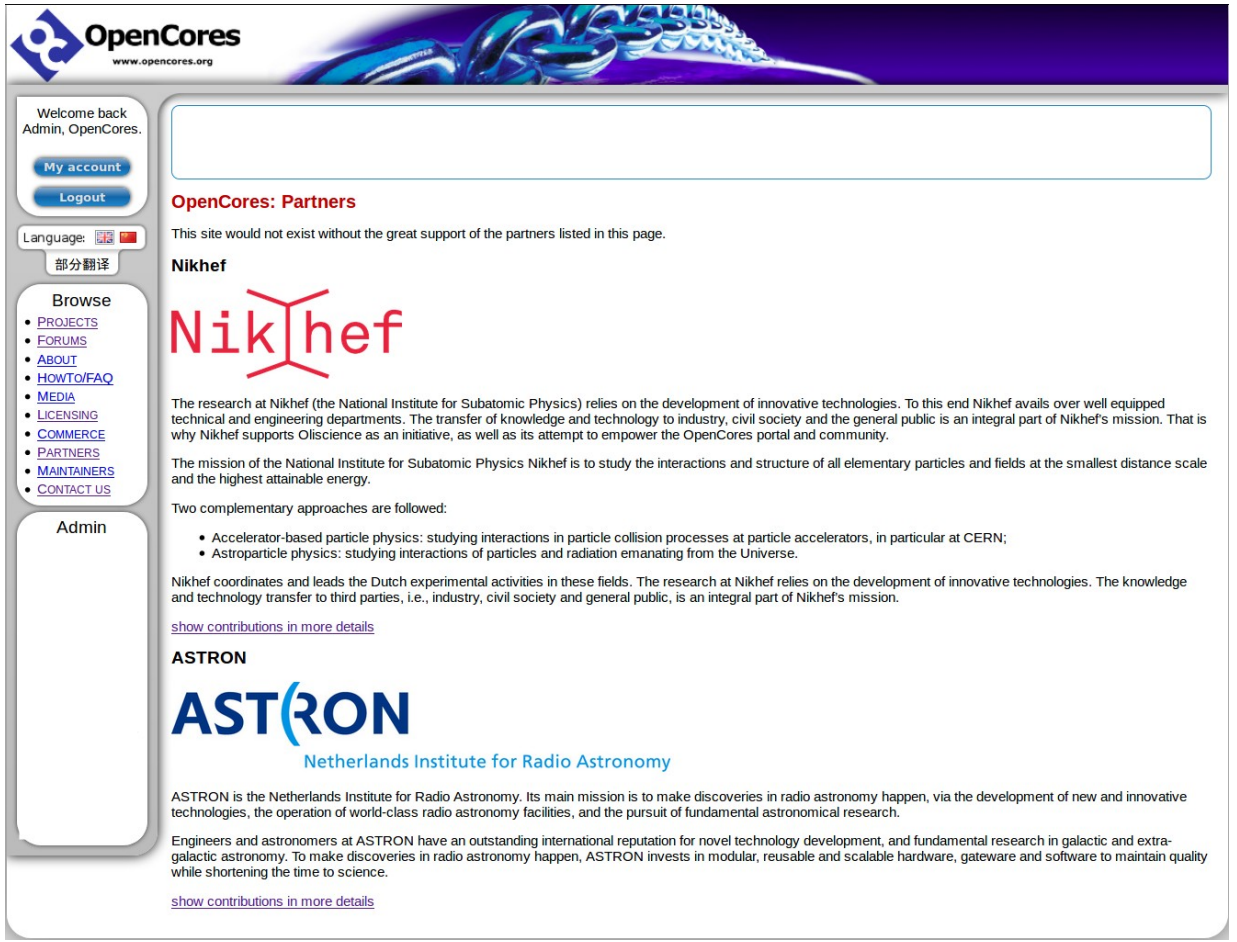
Share… why?

- Get the job done
- Avoid duplication effort
- Seeding of ideas
- Free peer review
- ***Sharing in the genes of scientific collaboration***
- A lot of testing done by third parties **(verification)**
- Promote common/good practices **(standardization)**
- Open Source is the future of gateware

OpenCores business advantage

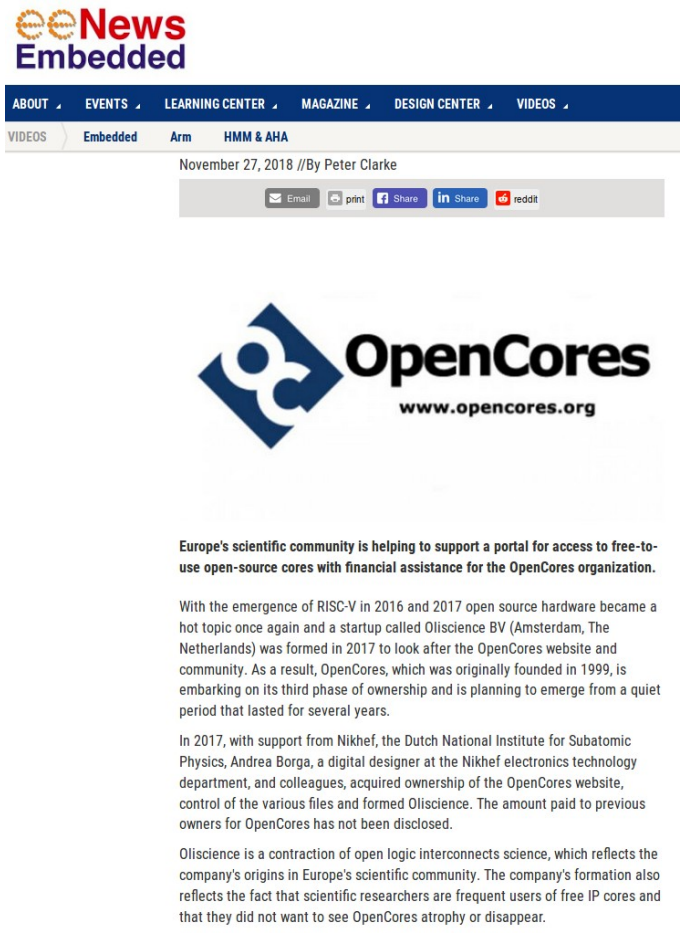
- **Community** to reach out and influence
  → knowledge is a great asset!
- **Marketing tool** targeting a specialized group
- **Market place** to engage potential customers
- **Human resource** to scout for talent

Premium partnership program



- **Freemium** model
- Higher **visibility** on the platform
- **Promotion** in the community
- **Influencing** new technology trends
- Indirect **marketing**

In the public domain



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November 27, 2018 //By Peter Clarke

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OpenCores
www.opencores.org

Europe's scientific community is helping to support a portal for access to free-to-use open-source cores with financial assistance for the OpenCores organization.

With the emergence of RISC-V in 2016 and 2017 open source hardware became a hot topic once again and a startup called Oliscience BV (Amsterdam, The Netherlands) was formed in 2017 to look after the OpenCores website and community. As a result, OpenCores, which was originally founded in 1999, is embarking on its third phase of ownership and is planning to emerge from a quiet period that lasted for several years.

In 2017, with support from Nikhef, the Dutch National Institute for Subatomic Physics, Andrea Borga, a digital designer at the Nikhef electronics technology department, and colleagues, acquired ownership of the OpenCores website, control of the various files and formed Oliscience. The amount paid to previous owners for OpenCores has not been disclosed.

Oliscience is a contraction of open logic interconnects science, which reflects the company's origins in Europe's scientific community. The company's formation also reflects the fact that scientific researchers are frequent users of free IP cores and that they did not want to see OpenCores atrophy or disappear.

- Open Cores rides again
- Honoured in OSDA program

Workshop on Open Source Design Automation (OSDA) 2019

held in conjunction with the Design, Automation and Test in Europe Conference (DATE)
Friday, March 29, 2019; Florence, Italy

Final Programme

Registration Link
Note: Please select "Friday Workshop W10"

Gratefully acknowledge support from our sponsors:

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Unspoken industry reference

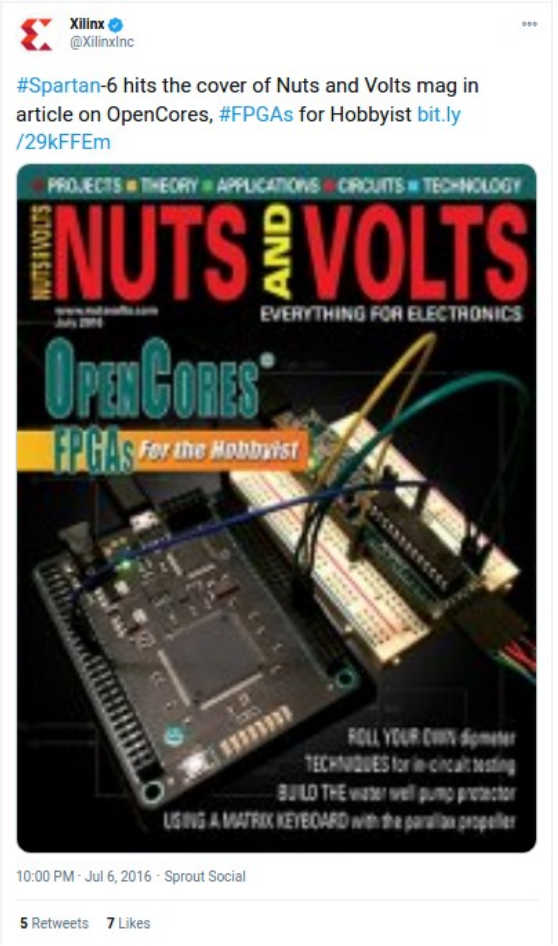


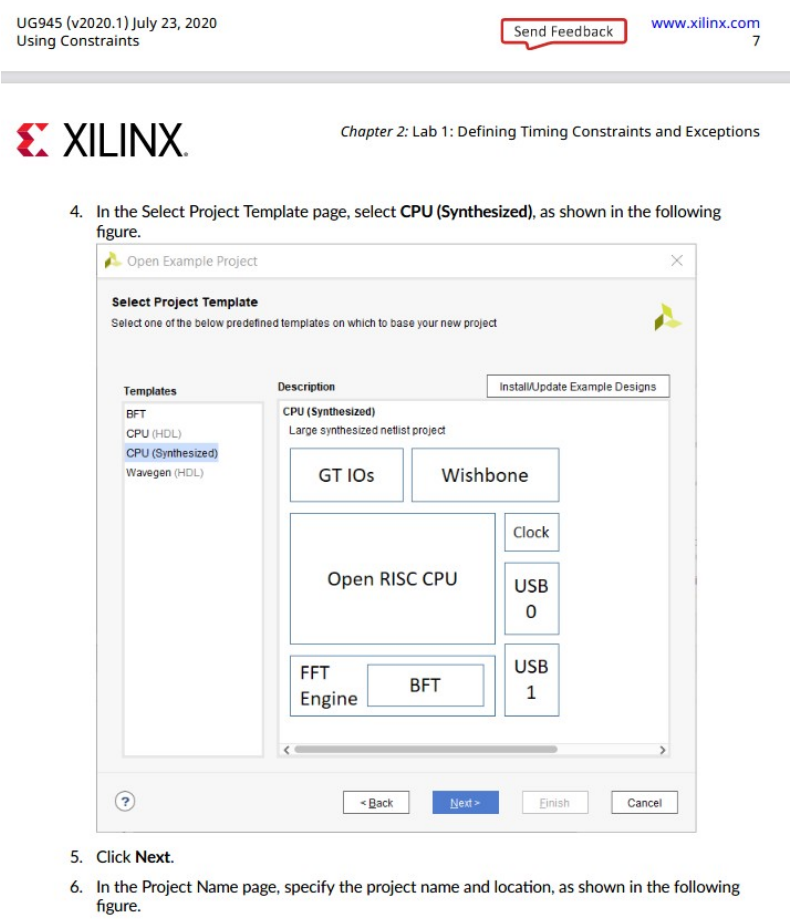
In today's world of big data, you need the highest performing FPGAs and SoCs. Intel® Arria® 10 devices provide up to 20% higher f_{MAX} than the competition, more than a speed grade advantage, as measured using publicly-available OpenCores designs.† Arria 10 devices are also the only 20 nm ARM*-based SoC with up to 1.5 GHz and hard floating-point digital signal processing (DSP) of up to 1.5 TFLOPS.†

Download our white paper, **Intel Arria 10 Performance Benchmarking Methodology and Results**, for detailed information on how Arria 10 devices beat the competition and provide the performance the market demands.

https://www.intel.com/content/www/us/en/programmable/b/arria-10-performance.html

Unspoken industry reference





Unspoken industry reference

Why Choosing the Right Design Tool Matters for Cost-Optimized FPGAs

amd_adaptivecomputing
Staff

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11-20-2024 08:30 AM

Editor's Note: This content is contributed by Maria Zaitchenko, Product Marketing Manager, AMD Cost-Optimized Portfolio Competitive Marketing.



AMD

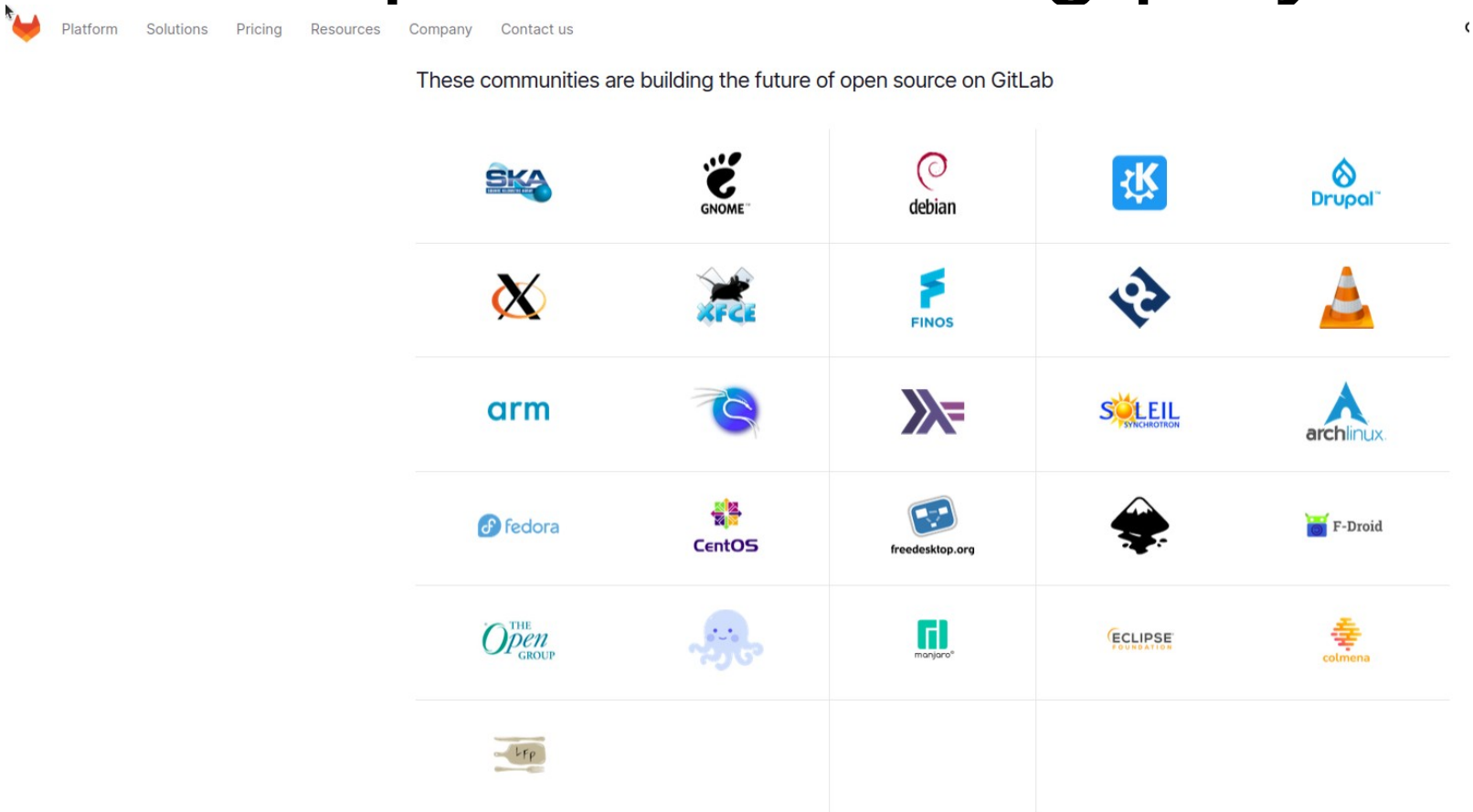
Maximizing Design Success with AMD Vivado Design Suite

Background of the Experiment

As a first step, we used 30 designs from OpenCores.org, ranging in size from a few hundred LUTs to a few thousand LUTs. These designs were compiled using AMD Vivado 2024.1 and Lattice Radiant 2024.1 with default tool settings. All benchmarks were conducted with the lowest speed grade devices (-1LV) from AMD, and the fastest speed grade from Lattice (-9 for Nexus and -3 for Avant). The rationale behind this match up is described in detail in WP558, *AMD FPGA Advantages over Competing Legacy LUT4 Architectures*. See Table 1 below for designs used in the experiment.

https://docs.amd.com/v/u/en-US/wp559-succeed-w-vivado

Open Source big player



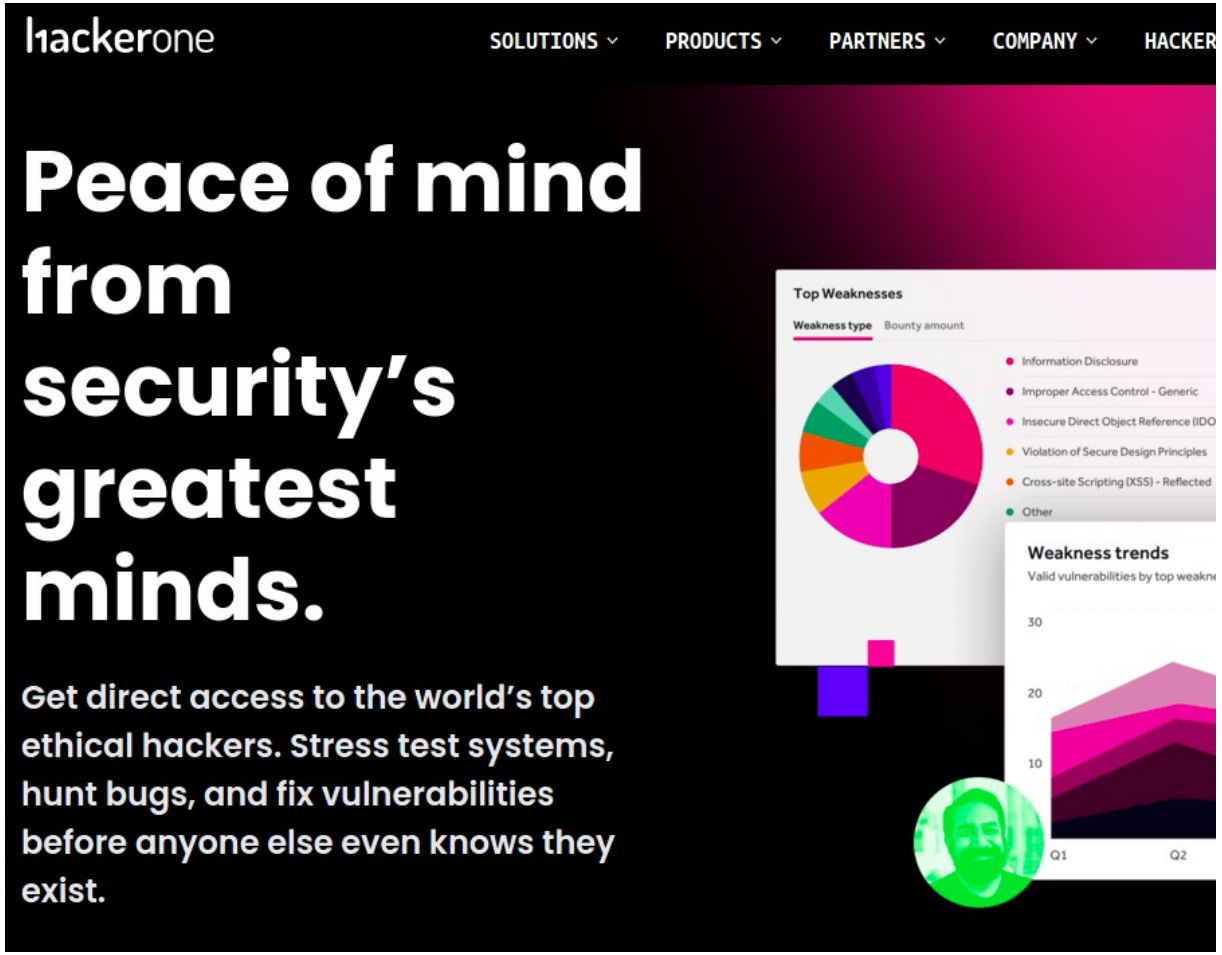
https://about.gitlab.com/solutions/open-source/partners/

Future oriented



https://about.gitlab.com/blog/2019/12/03/welcoming-opencores-to-gitlab/

Future oriented



- Bring **hacking** spirit to the semiconductor industry
- **Bug bounty** challenges
- **Paid rewards** as incentives
- **Proven business model** for the software world

Ambitious Ambitions

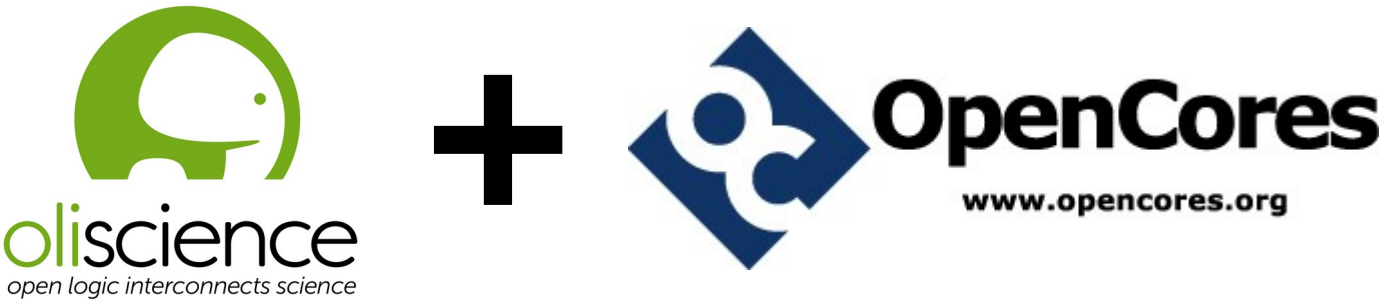
- we are self sufficient but...
- **...we would like to grow further and faster!**
- Research world supportive but not enough
- Tackle technology challenges
  - → modernize platform
  - → improve content quality
  - → improve content diversity
- Broaden footprint and reach



Opportunities for SMEs

- Global visibility
- Competitive advantage for marketing
  → relevant target markets
- Engage key players in the field!
- Access to specialized resources
  → digital designers' contributions
  → receptive users' space

Thank you



www.opencores.org
www.oliscience.nl
LinkedIn: https://www.linkedin.com/company/oliscience/
Twitter: @Oliscience101

Backup slides



Another fundamental aspect

What is valorisation?

Valorisation is defined and applied in various ways.

Policymakers like the VSNU, Rathenau, Advisory Council for Science, Technology and Innovation (AWT), and NWO define 'valorisation' as follows:

'Valorisation is the process of creating value from knowledge, by making knowledge suitable and available for societal and/or economic application and by transforming it into products, services, processes and new business.'

Premium partner

Nikhef



"[…] **The transfer of knowledge and technology to industry, civil society and the general public is an integral part of Nikhef's mission**. That is why Nikhef supports Oliscience as an initiative, as well as its attempt to empower the OpenCores portal and community." - *Jan Visser*

https://www.nikhef.nl/news/first-cern-bic-nikhef-start-up-is-launched/

Premium partner

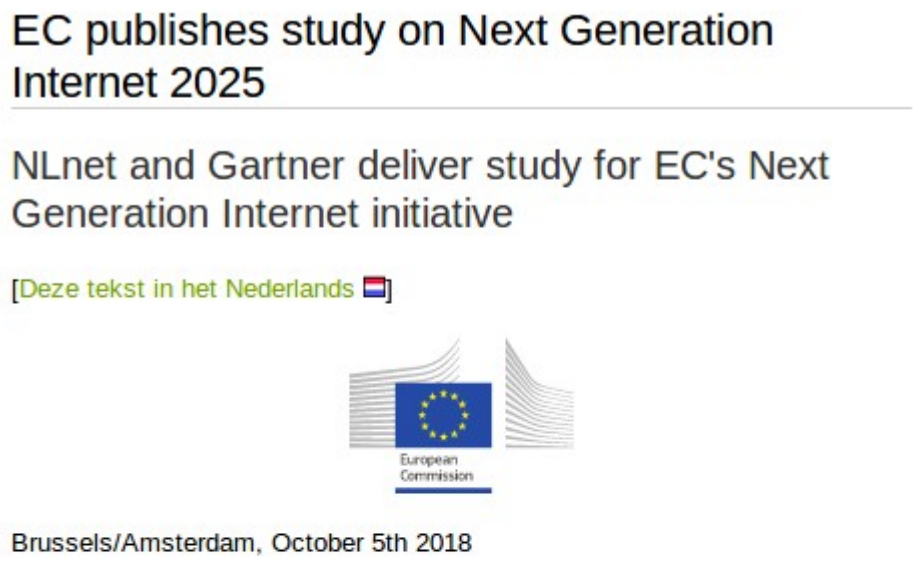
ASTRON
Netherlands Institute for Radio Astronomy

"[…] **We are working on the opposite extremes of physics, but we are using the same technology**. This collaboration allows us to share ideas and reuse FPGA designs, which will help to speed-up the process of engineering the tools for science."- *Daniel Van der Schuur*



In the public domain

- Mentioned in a report for the EU Commission…



EC publishes study on Next Generation Internet 2025

NLnet and Gartner deliver study for EC's Next Generation Internet initiative

[Deze tekst in het Nederlands]

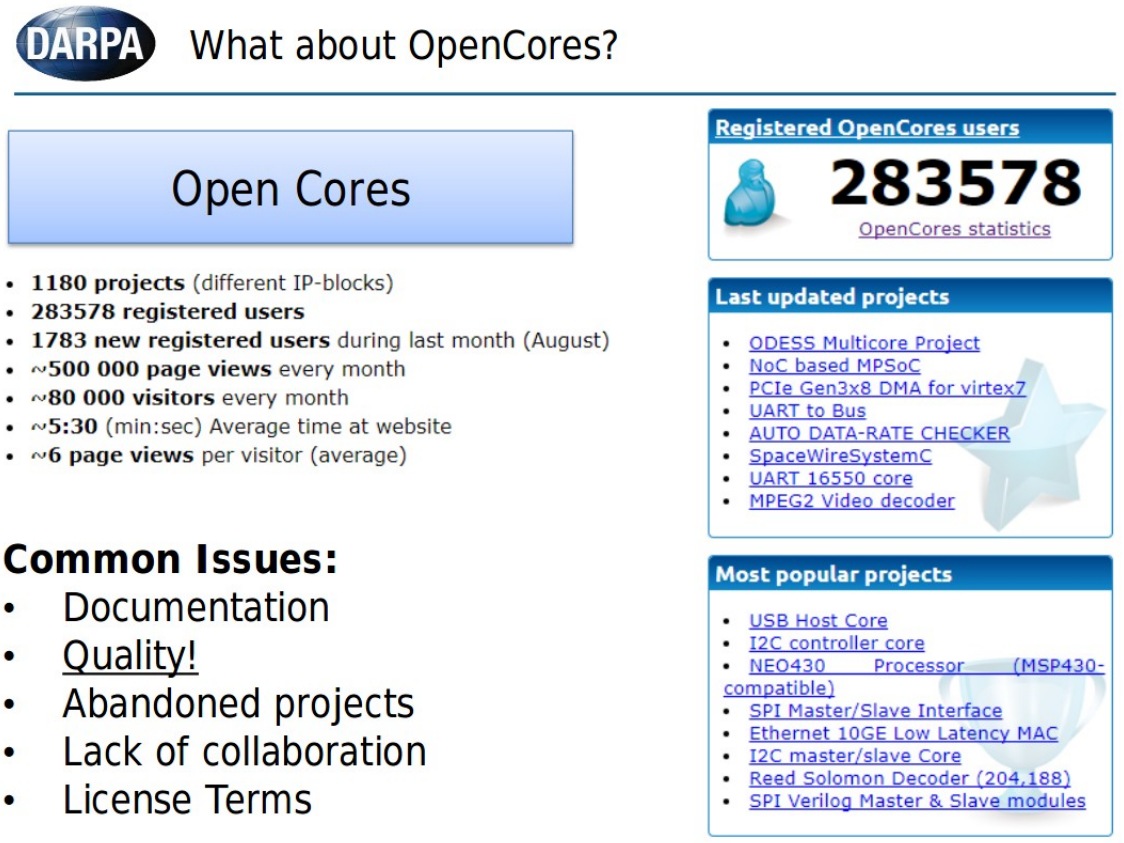
European Commission

Brussels/Amsterdam, October 5th 2018

https://nlnet.nl/news/2018/20181005-NGI-Study-Report-en.html

In the public domain

- … and DARPA (US)



https://www.darpa.mil/attachments/eri_design_proposers_day.pdf