

FPGA as a multidisciplinary tool for scientific research and industry

a practical example

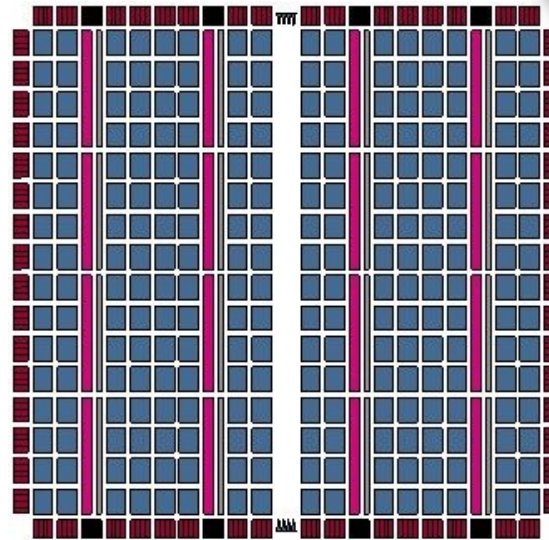
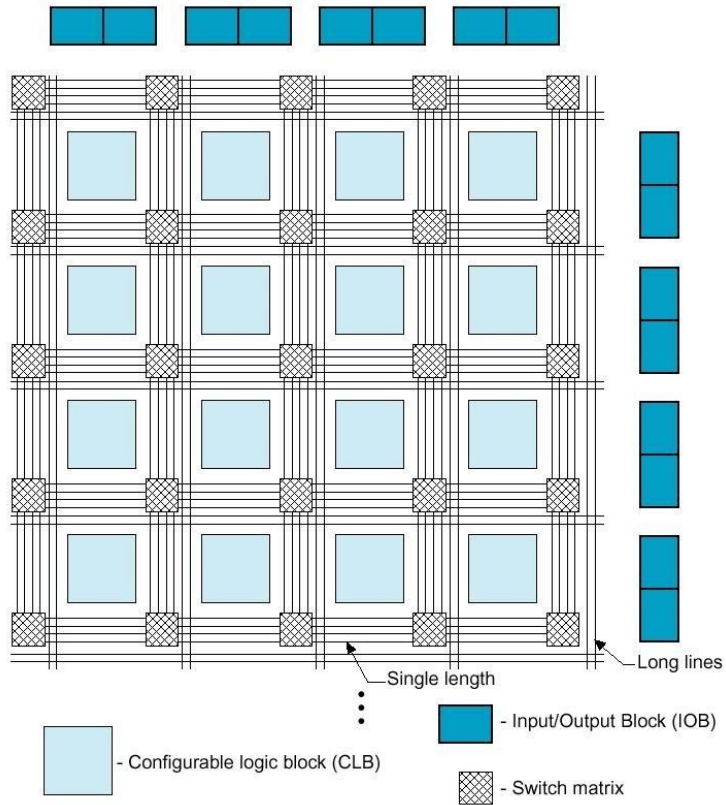
Andrea Borga

digital design engineer and co-founder

Outlook

- Setting the scene: FPGA
- Nikhef and its activities
- Sharing development efforts
- Technology forecast
- Open Source initiatives at CERN
- Oliscience in a nutshell
- OpenCores
- Closing thoughts

FPGA



- Slices
- Block RAM
- Dedicated multiplier
- I/O Block
- DCM
- Clock buffer

<http://www.xilinx.com>

<http://www.altera.com>

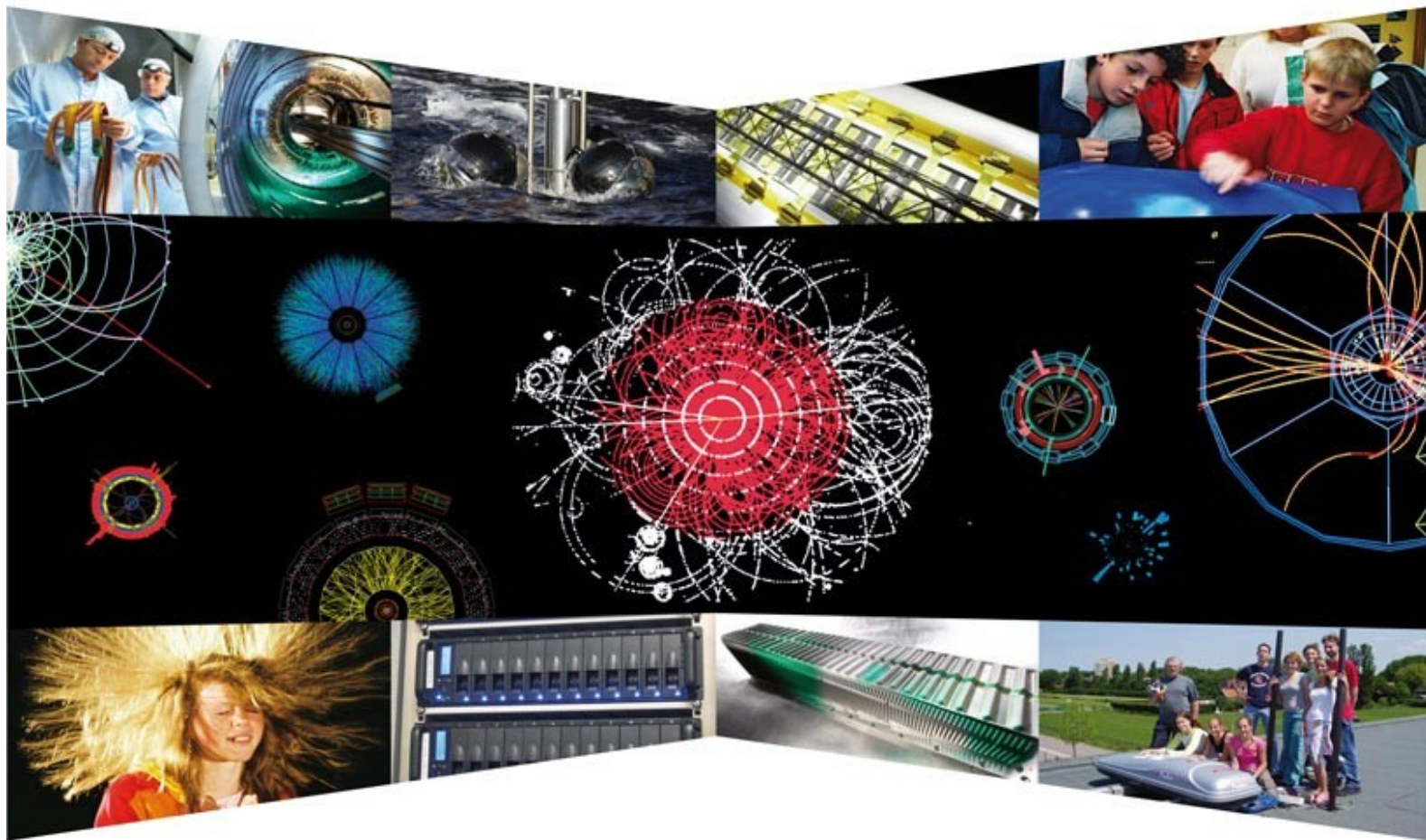
FPGA in research and industry

andy@oliscience.nl

Filling enormous FPGA



About Nikhef

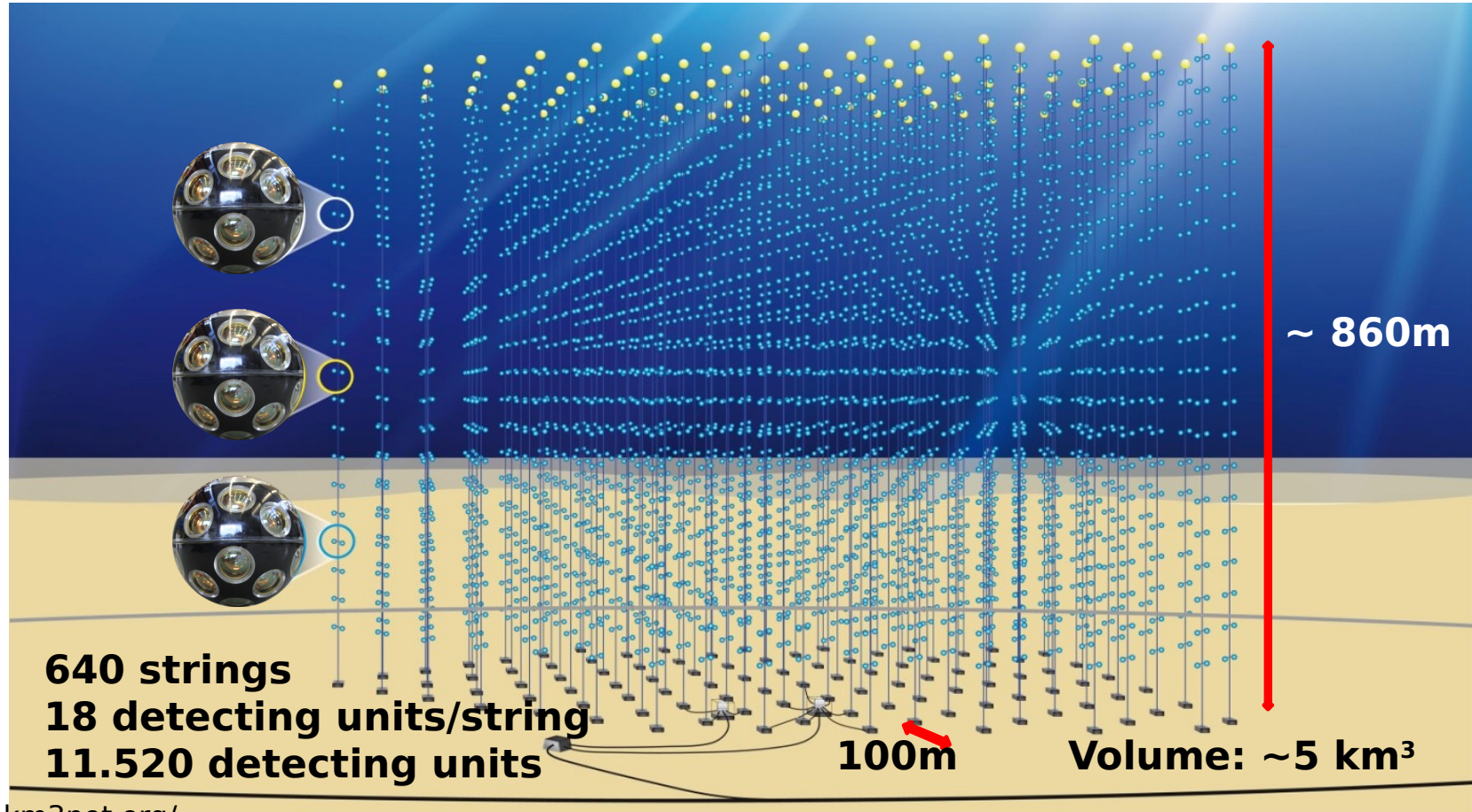


Astroparticle physics



P.C. Budassi, "Observable universe on a log scale" (2016)

Astroparticle physics: Km3Net

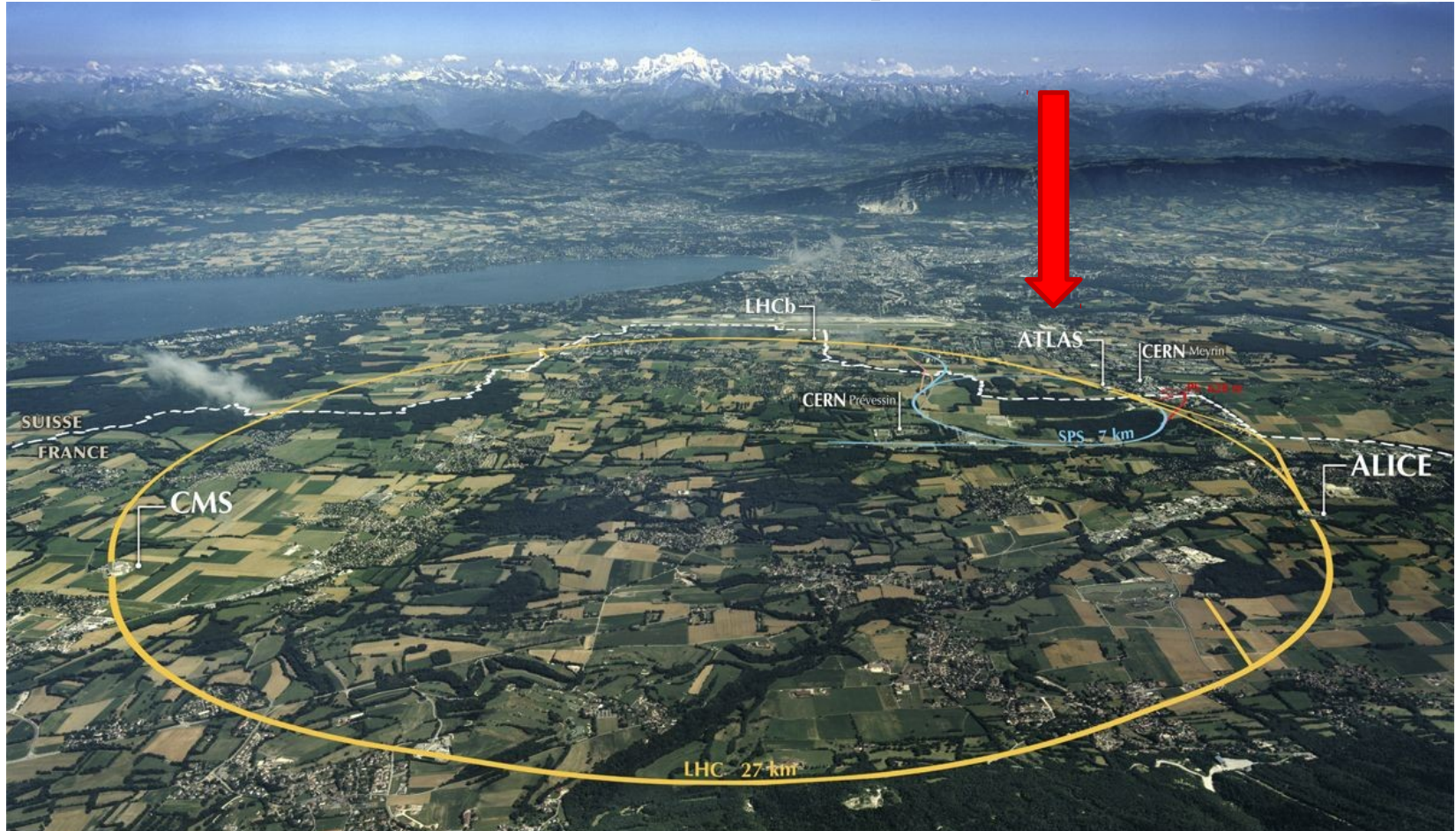


Accelerator physics: CERN LHC

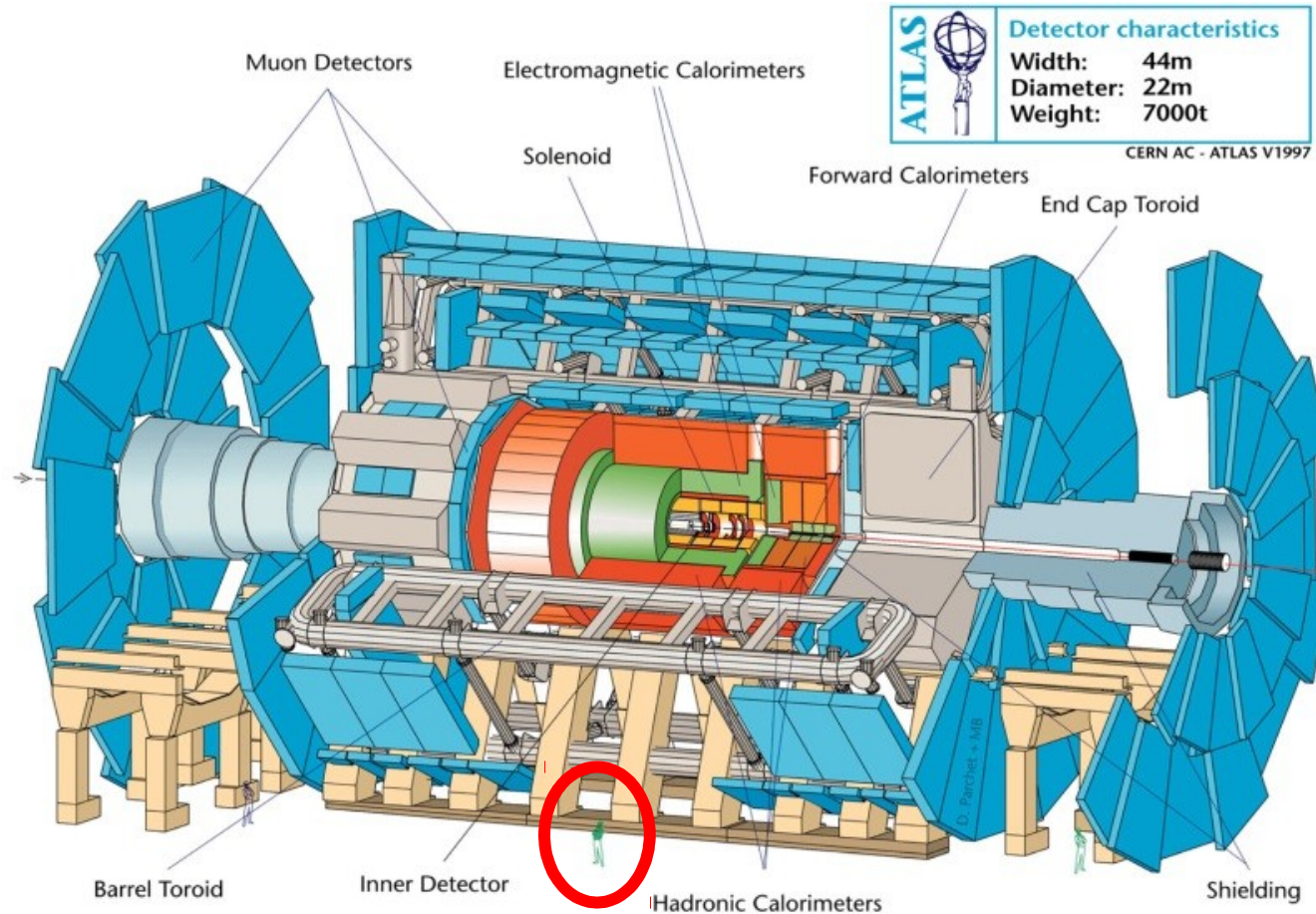


<http://www.cern.ch>

CERN ATLAS Experiment

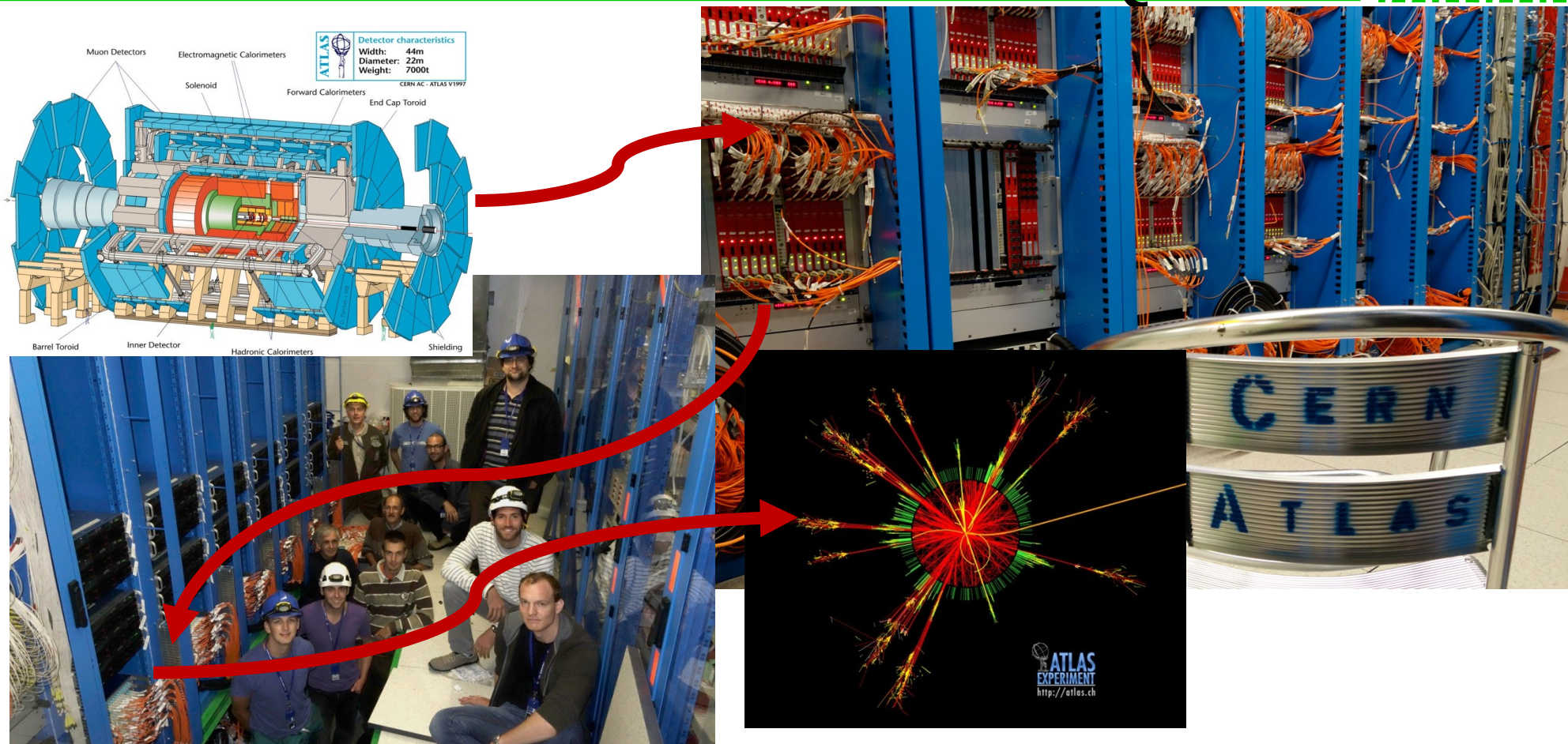


CERN ATLAS detector

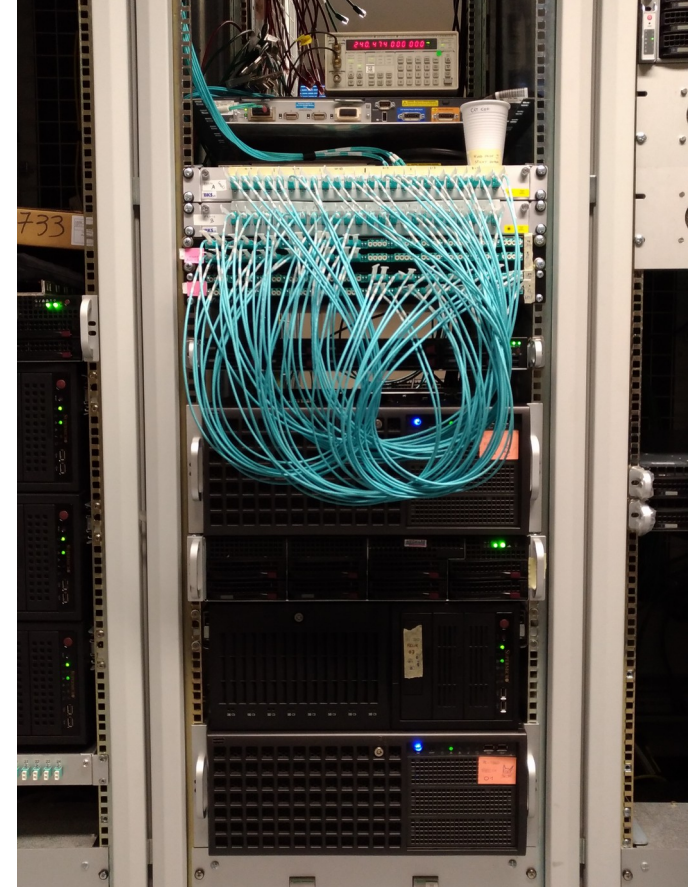
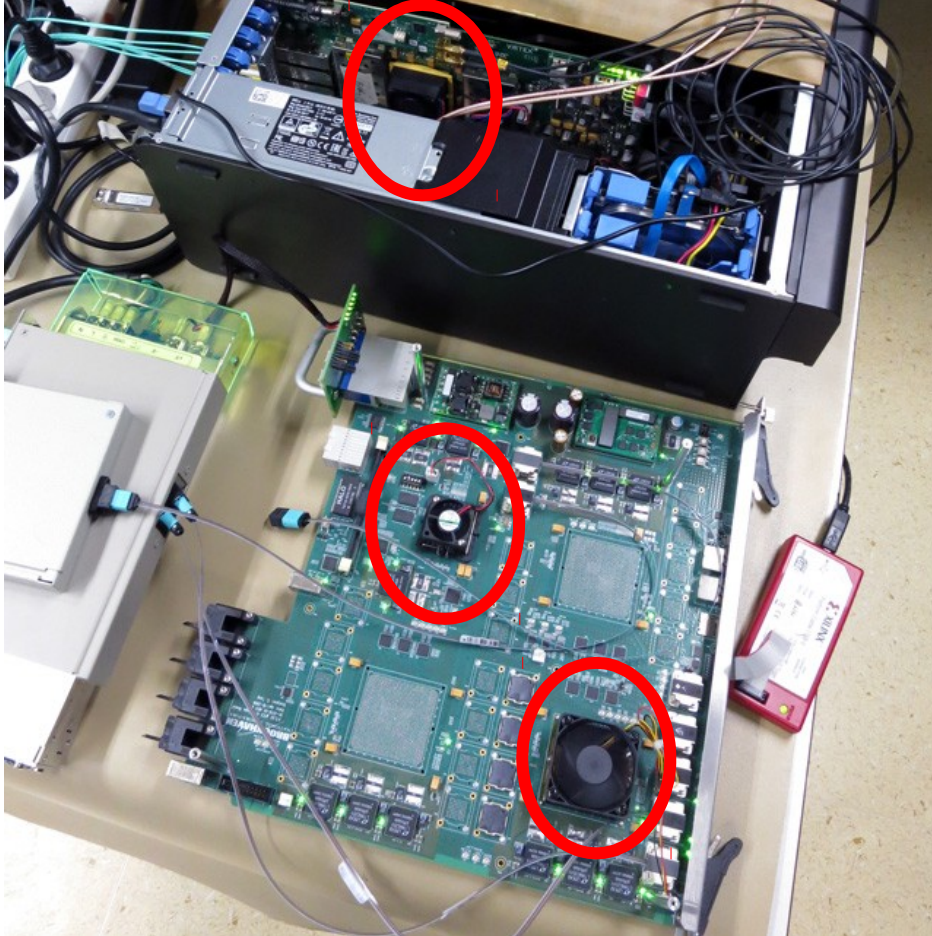


<http://atlas.cern>

CERN ATLAS DAQ



FPGA in DAQ systems



<https://atlas-project-felix.web.cern.ch/>

andy@oliscience.nl

At the heart of the matter

★ Wupper: PCIe DMA Engine for Xilinx FPGAs :: Overview

Overview

Hardware details

Software details

Doxygen

News

Downloads

Bugtracker

Edit pages

Add a block

Define block order

Help

Details

Name: virtex7_pcie_dma

Created: Dec 18, 2014

Updated: Apr 7, 2018

SVN Updated: Feb 14, 2018

SVN: [Browse](#)

Latest version: [download](#) (might take a bit to start...)

Statistics: [View](#)

[Bugs](#): 7 reported / 6 solved

★ Unstar 8 you like it: star it!

Other project properties EDIT

Category: [System controller](#)

Language: [VHDL](#)

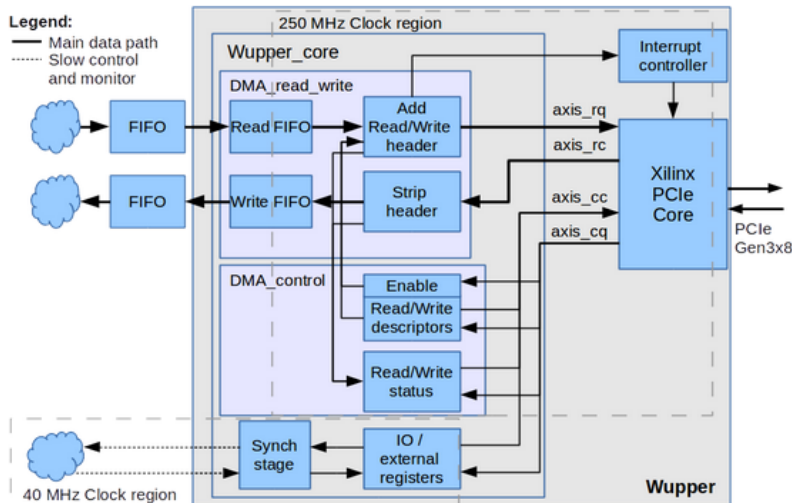
Development status: [Mature](#)

Additional info: [FPGA proven](#), [Specification done](#)

WishBone compliant: No

WishBone version: n/a

License: LGPL



WUPPER



Project maintainers

- [Borga, Andrea](#)
- [Blankers, Roel](#)
- [Schreuder, Frans](#)
- [Kharraz, Oussama](#)
- [Add maintainer](#)

Partner team

Nikhef

✉ nikhef@opencores.org

At the heart of the matter

YAML

```
MINI_EGROUP_CTRL:-
  number: 24
  format_name: MINI_EGROUP_CTRL
  entries:-
    name: EC_TOHOST
    format_name: EC_TOHOST_{index:02}
    type_name: EC_TOHOST
    desc: Configures the ToHost Mini egroup in EC mode
    type: W
    bitfield:
      range: 2..1
      name: ENCODING
      desc: Configures encoding of the EC channel
      default: 0x2
      range: 0
      name: ENABLE
      desc: Enables the EC channel
      default: 1
      name: EC_FROMHOST
```



C++

```
// MINI_EGROUP_CTRL
{ REG_EC_TOHOST_00,
  "Full Register",
  0x02780,
  REGMAP_REG_READ|REGMAP_REG_WRITE
},
{ REG_EC_FROMHOST_00,
  "Full Register",
  0x02710,
  REGMAP_REG_READ|REGMAP_REG_WRITE
},
{ REG_TTC_TOHOST_00,
  "Full Register",
  0x02720,
  REGMAP_REG_READ|REGMAP_REG_WRITE
},
{ REG_EC_TOHOST_01,
  "Full Register",
  0x02730,
  REGMAP_REG_READ|REGMAP_REG_WRITE
},
}
```

L^AT_EX

MINI_EGROUP_CTRL						
0x2700	0,1	EC_TOHOST_00	ENCODING	2:1	W	Configures encoding of the EC channel Enables the EC channel
			ENABLE	0	W	
0x2710	0,1	EC_FROMHOST_00	ENCODING	4:1	W	Configures encoding of the EC channel Configures the FromHost Mini egroup in EC mode
			ENABLE	0	W	
0x2720	0,1	TTC_TOHOST_00		0	W	Enables the ToHost Mini Egroup in TTC mode

VHDL

```
---** MINI_EGROUP_CTRL
constant REG_EC_TOHOST_00 : std_logic_vector(19 downto 0) := x"02780";
constant REG_EC_FROMHOST_00 : std_logic_vector(19 downto 0) := x"02710";
constant REG_TTC_TOHOST_00 : std_logic_vector(19 downto 0) := x"02720";
constant REG_EC_TOHOST_01 : std_logic_vector(19 downto 0) := x"02730";
constant REG_EC_FROMHOST_01 : std_logic_vector(19 downto 0) := x"02740";
constant REG_TTC_TOHOST_01 : std_logic_vector(19 downto 0) := x"02750";

when REG_EC_FROMHOST_00 => register_map_control_s.EC_FROMHOST_00.ENCODING <= register_write_data_40_s(4 downto 1); -- Configures encoding of the EC channel
when REG_EC_FROMHOST_00 => register_map_control_s.EC_FROMHOST_00.ENABLE <= register_write_data_40_s(0 downto 0); -- Configures the FromHost Mini egroup in EC mode
when REG_TTC_TOHOST_01 => register_map_control_s.EC_TOHOST_01.ENCODING <= register_write_data_40_s(2 downto 1); -- Enables the ToHost Mini Egroup in TTC mode
when REG_TTC_TOHOST_01 => register_map_control_s.EC_TOHOST_01.ENABLE <= register_write_data_40_s(0 downto 0); -- Enables the EC channel
when REG_EC_FROMHOST_01 => register_map_control_s.EC_FROMHOST_01.ENCODING <= register_write_data_40_s(4 downto 1); -- Configures encoding of the EC channel
when REG_EC_FROMHOST_01 => register_map_control_s.EC_FROMHOST_01.ENABLE <= register_write_data_40_s(0 downto 0); -- Configures the FromHost Mini egroup in EC mode
when REG_TTC_TOHOST_01 => register_map_control_s.TTC_TOHOST_01 <= register_write_data_40_s(0 downto 0); -- Enables the ToHost Mini Egroup in TTC mode
when REG_EC_TOHOST_02 => register_map_control_s.EC_TOHOST_02.ENCODING <= register_write_data_40_s(2 downto 1); -- Configures encoding of the EC channel
when REG_EC_TOHOST_02 => register_map_control_s.EC_TOHOST_02.ENABLE <= register_write_data_40_s(0 downto 0); -- Enables the EC channel
```

FPGA upcoming challenges

- complexity is exponentially growing
→ we already struggle to keep up
- FPGA are no more what they used to be
gate arrays → full SoC → beyond
- access to hardware description needs
new development approaches
- new dev-skill sets to be devised and taught
- and... we should stop reinventing the wheel...

Share is the name game

Share... why?

- Get the job done
- Avoid duplication effort
- Seeding of ideas
- Free peer review
- A lot of testing done by third parties
- Sharing often comes bidirectional
- The sum is more than 1



CERN efforts

to share...
or...
to share more!

Javier Serrano from CERN



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OPEN HARDWARE REPOSITORY

[SIGN IN](#) [REGISTER](#)



PROJECTS



FEATURED PROJECTS

CERN BE-CO-HT contribution to KiCad

This project hosts documentation and code to be contributed by CERN's BE-CO-HT section to the KiCad PCB design tool.

[More info at the Wiki page](#)

CERN Open Hardware Licence

A project devoted to developing and discussing the CERN Open Hardware Licence.

[More info at the Wiki page](#)

FMC ADC 100M 14b 4cha

FmcAdc100M14b4cha is a 4 channel 100MSPS 14 bit ADC low pin count FPGA Mezzanine Card (VITA 57). Input ranges: +/-50mV, +/-0.5V, +/-5V. The offset correction by +/- 5V is possible for each gain range. Commercially available.

[More info at the Wiki page...](#)

FMC DEL 1ns 4cha

Welcome

Welcome to the Open Hardware Repository, a place on the web for electronics designers at experimental physics facilities to collaborate on open hardware designs, much in the philosophy of the free software movement. You can get more details about our vision by reading [our manifesto](#).

- Browse the [Projects list](#)
- Read about the [Open Hardware Repository](#)
- Check out the [CERN Open Hardware Licence](#)
- Visit the [Getting Started page](#)

If you need further assistance, or detect a problem with the site, please open a [support ticket](#).

Latest news

OHR Meta Project: "Open Hardware and Collaboration"

as Keynote presentation at PCaPAC.

Added by [Erik van der Bij](#) on [25 Oct 2016 at 10:24](#)

<http://www.ohwr.org>

FPGA in research and industry

andy@oliscience.nl

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HOME PROJECTS LICENSES COMPANIES

SIGN IN REGISTER

CERN OPEN HARDWARE LICENCE

OVERVIEW

WIKI

ACTIVITY

MAILING LIST

NEWS

DOCUMENTS

CERN Open Hardware Licence - Introduction

Myriam Ayass, legal adviser of the Knowledge and Technology Transfer Group at CERN and author of the CERN OHL:

In the spirit of knowledge sharing and dissemination, the CERN Open Hardware Licence (CERN OHL) governs the use, copying, modification and distribution of hardware design documentation, and the manufacture and distribution of products.

*The CERN-OHL is to hardware what the General Public Licence (GPL) is to software. It defines the conditions under which a licensee will be able to use or modify the licensed material. The concept of 'open-source hardware' or 'open hardware' is not yet as well known or widespread as the free software or open-source software concept. However, it shares the same principles: **anyone should be able to see the source (the design documentation in case of hardware), study it, modify it and share it.***

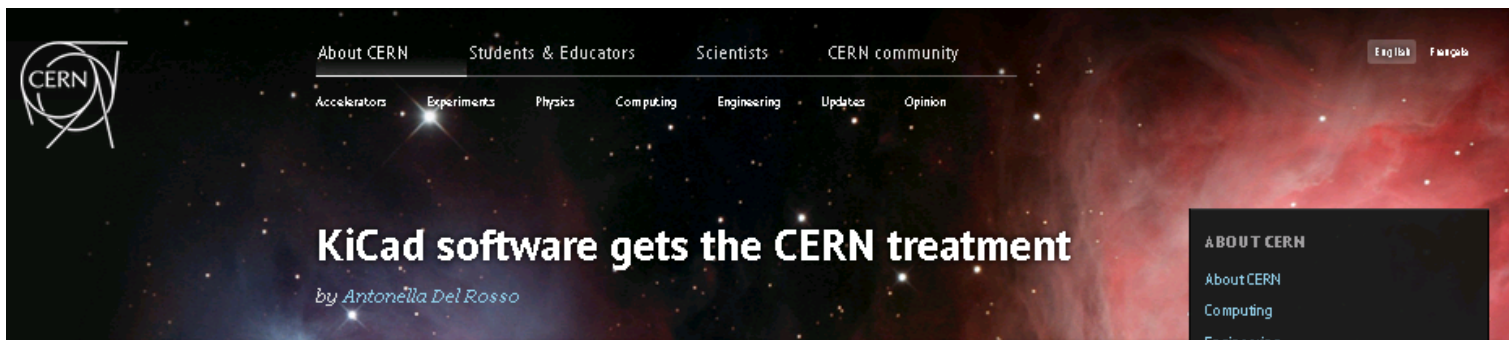
In addition, if modifications are made and distributed, it must be under the same licence conditions – this is the 'persistent' nature of the licence, which ensures that the whole community will continue benefiting from improvements, in the sense that everyone will in turn be able to make modifications to these improvements.

History

Wiki

[Start page](#)
[Index by title](#)
[Index by date](#)

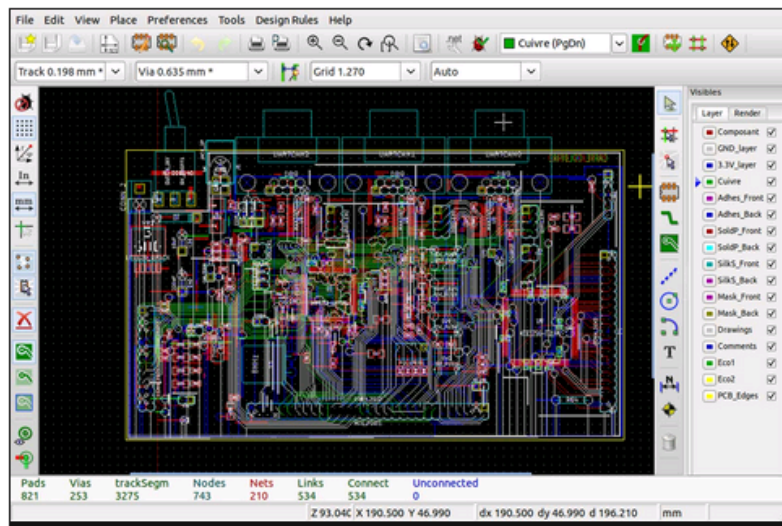
CERN efforts



Posted by [Cian O'Lunaigh](#) on 17 Feb 2015. Last updated 18 Feb 2015, 10.06.

[Voir en français](#)

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[Experiments](#)
[How a detector works](#)

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CERN UPDATES

[A new ring to slow down antimatter](#)

28 Nov 2016

[Meet TIM, the LHC tunnel's robot](#)

25 Nov 2016

[NA64 hunts the mysterious dark photon](#)

25 Nov 2016

[more updates >](#)



oliscience
open logic interconnects science

Oliscience team

- **Alberto Alberton: (sales and marketing)**
 - experienced entrepreneur
 - angel investor in oliscience
- **Leo Davoli: (legal and operations)**
 - professional lawyer
 - angel investor in oliscience
- **Andrea Borga: (CEO and CTO)**
 - seasoned digital design engineer
 - passionate technologist
 - open source enthusiast
 - the geek!



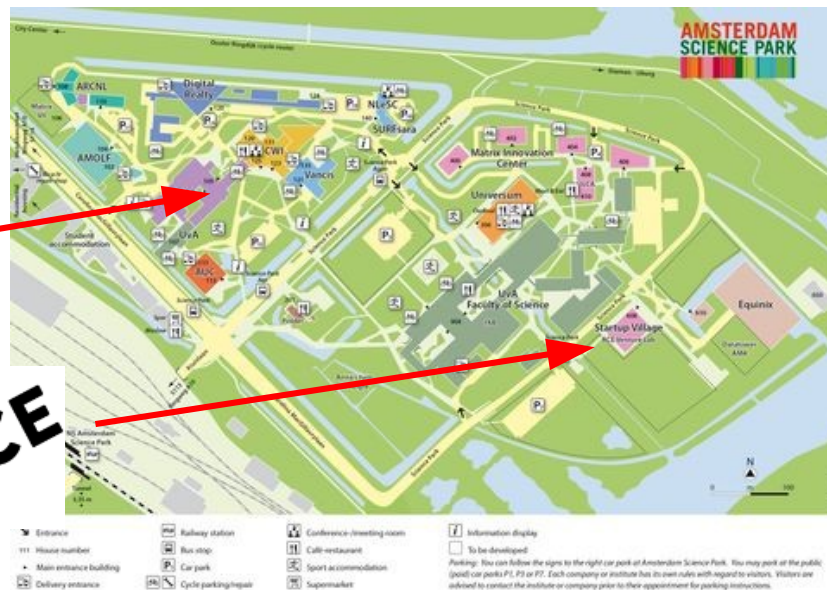
About Oliscience

- Originating from the CERN-BIC at Nikhef

Nikhef

- Coached at Amsterdam
Centre for Entrepreneurship
- Based at the Amsterdam Science Park

ACE



Oliscience in a nutshell

- Core business: FPGA technology
- Providing consultancy services
- Innovating in the field of FPGA technology
- Driving the OpenCores.org platform: portal for the exchange of open source IP

The “good old” OpenCores.org



The screenshot shows the OpenCores.org website in a Chromium browser window. The page features a navigation sidebar on the left with links for Projects, Forums, About, HowTo/FAQ, Media, Licensing, Commerce, Partners, Maintainers, and Contact Us. The main content area includes a login/register section, a 'What is OpenCores?' section describing the community, and several project highlights. A 'Professional support' section at the bottom promotes Oliscience's services.

OpenCores
www.opencores.org

Username:
Password:
☐ Remember me
[Login](#)
[Register](#)

Language:  部分翻译

Browse

- [PROJECTS](#)
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- [MEDIA](#)
- [LICENSING](#)
- [COMMERCE](#)
- [PARTNERS](#)
- [MAINTAINERS](#)
- [CONTACT US](#)

Tools
Google Custom S

What is OpenCores?


The reference community for Free and Open Source gateway IP cores

Since 1999, OpenCores is the most prominent online community for the development of gateway IP (Intellectual Properties) Cores. It is the place where such cores are shared and promoted in the spirit of Free and Open Source collaboration.

The OpenCores portal hosts the source code for different digital gateway projects and supports the users' community providing a platform for listing, presenting, and managing such projects; together with version control systems for sources management.

OpenCores is also the place where digital designers meet to showcase, promote, and talk about their passion and work. They do this through forums, news collectors, and much more!

Please join us!

Registered OpenCores users

300000
[OpenCores statistics](#)

Last updated projects

- [Attiny Atmega Xmega core](#)
- [lon - MIPS\(tm\) compatible CPU](#)
- [SHA3 \(KECCAK\)](#)
- [APB to I2C](#)
- [Floating Point Adder and Multiplier](#)
- [NextZ80](#)
- [cpu65c02_ic - R65C02 Processor Soft Core with accurate timing](#)
- [T80 cpu](#)

Most popular projects


- [802.3an LDPC Decoder](#)
- [I2C controller core](#)
- [OpenRISC 2000](#)
- [SPI Master/Slave Interface](#)
- [APB to I2C](#)
- [SPI Verilog Master & Slave modules](#)
- [PWM](#)
- [I2C master/slave Core](#)

Projects


[Browse all Projects \(Cores\)](#)

Forum

[Communicate in the forums](#)

WebShop

[Visit our Webshop](#)

Professional support


oliscience
open logic interconnects science

We are the developers and maintainers of this website and community, but not only!
If you plan to use IP Cores from OpenCores in your next design and need support, or if you require professional advise on your next challenging IP Core development, don't hesitate to contact us.

We are experts in gateway design and engineering based on the OpenCores technology, and have extensive experience in all parts of FPGA development.
Please visit [Oliscience](#) for further information and enquiries.

OpenCores.org in numbers

- Funded in 1999
- Frequented by >300.000 professionals
- Generating ~500.000 views per month
- **Acquired by Oliscience in 2017**
- Steadily increasing activity [up 30% from acquisition]
- Still strong identity, established trademark, consistent community, very specialized

OpenCores.org purpose

- OpenCores brings together Digital Design Engineers
- access to specialized developers
 - OpenCores offers precious insights
 - OpenCores pushes the frontier of possibilities
- **make FPGA and gateware more accessible**
- **push!** ensure that the best IP blocks are used and let them be improved further by the community
- **pull!** encourage more people to add their IP cores

Oliscience goals

- **Stimulate** the community
- **Offer** an “impact metrics” to asses performance
- **Motivate** designers to contribute
- **Offer** a forum for like-minds to meet
- **Promote** best-in-class design practices
- **Provide consultancy services via the portal in the field of gateway design and support**

A call to action to partners

**we develop, drive and promote
the large OpenCores community**

consisting of:

- Research institutions
- Universities
- High-tech corporates

**you access resources on our portal
and contribute fostering common practices**

OpenCores → to the next level.....

- Grow community and increase content
 - many micro processors architectures
 - virtually all standard peripherals
 - a lot of general infrastructure cores
- Explore new fields
 - High Level Synthesis languages, complex SoC systems
 - Data Centres, HPC clusters, hardware acceleration

**be the reference market place where
new ideas are exchanged and advanced**

Premium partner

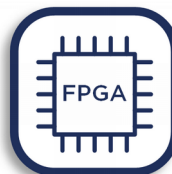
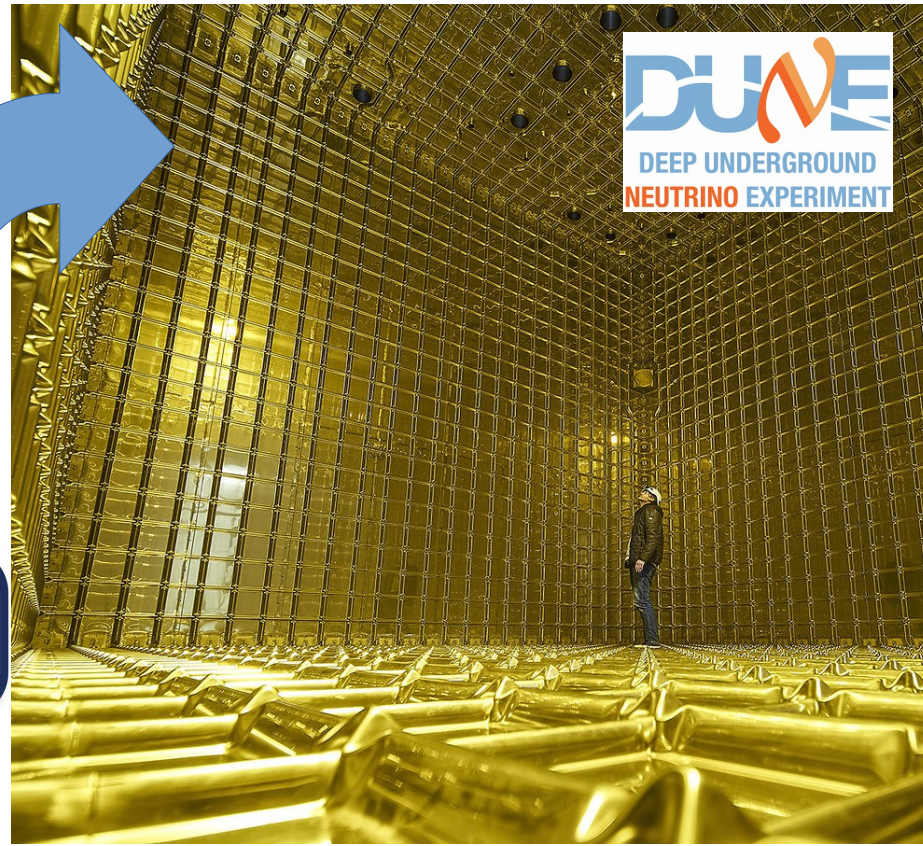
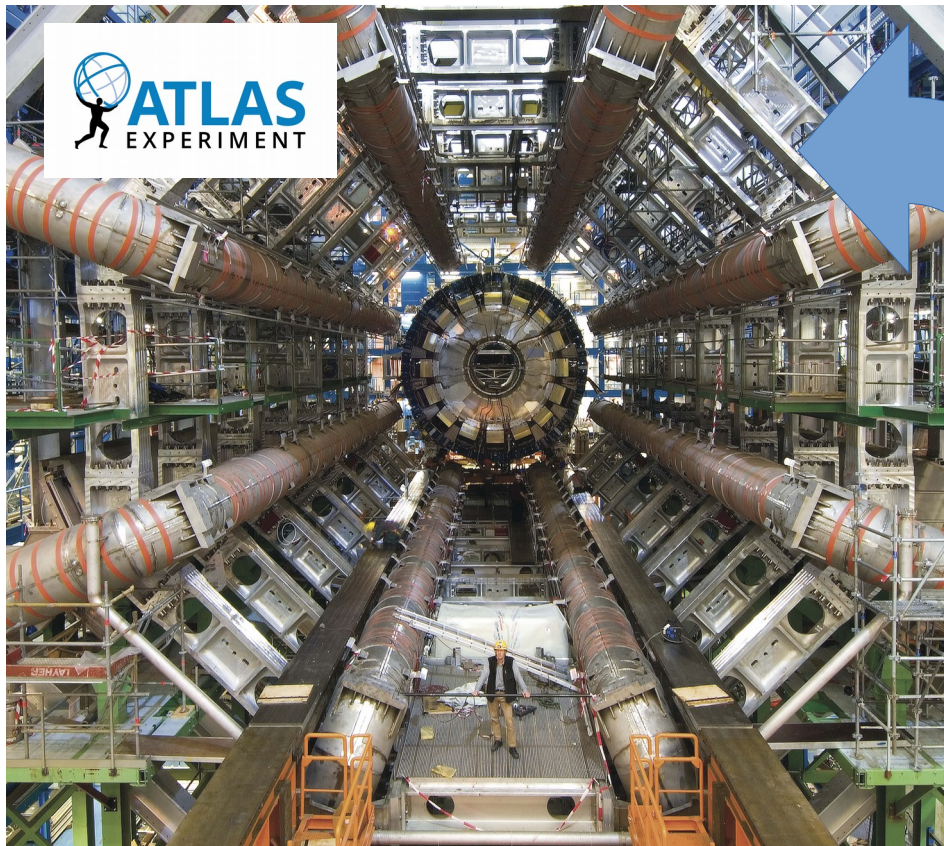
ASTRON

Netherlands Institute for Radio Astronomy

“[...] We are working on the opposite extremes of physics, but we are using the same technology. This collaboration allows us to share ideas and reuse FPGA designs, which will help to speed-up the process of engineering the tools for science.”- *Daniel Van der Schuur*

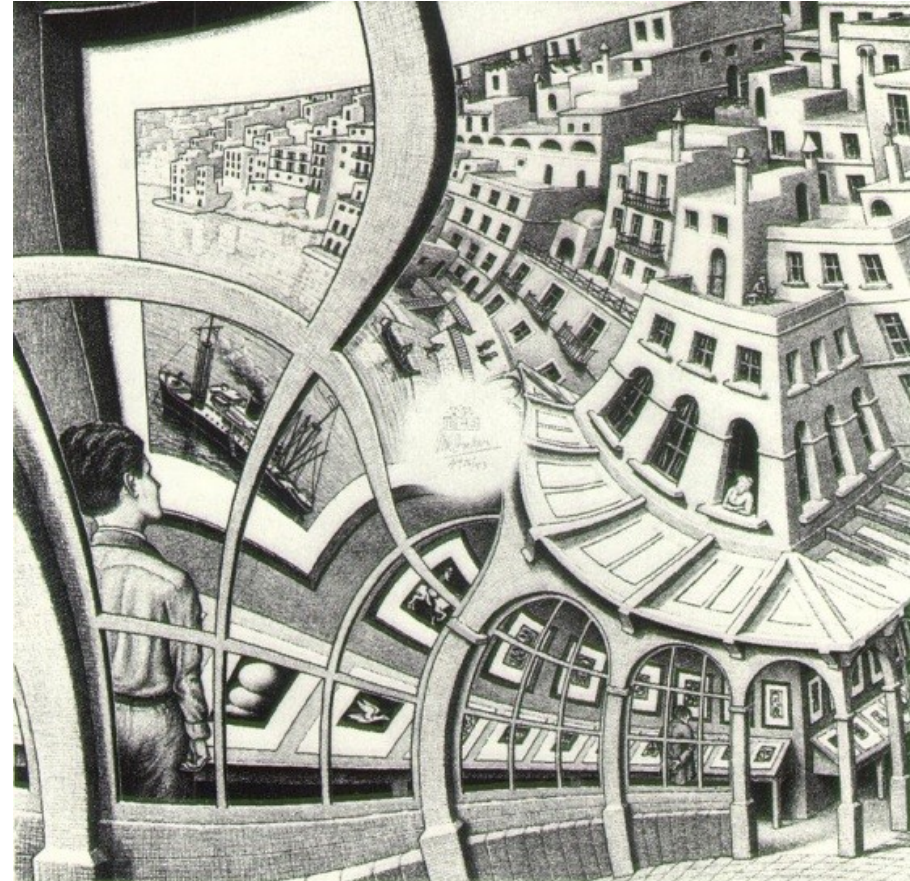


Consultancy customer



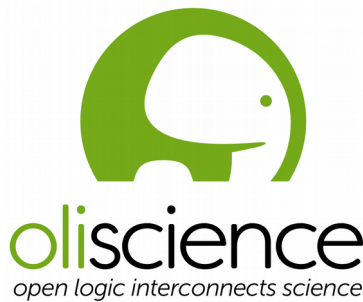
Think different future perspectives

- Fight “engineering inertia”
 - look for changes
- Embrace and engage
 - look for alliances
- Cross-contaminate
 - dare to share



M.C. Escher, "Prententoonstelling" (1956)

Thank you



+



OpenCores

www.opencores.org

www.opencores.org

www.oliscience.nl

LinkedIn: <https://www.linkedin.com/company/oliscience/>

Twitter: @Oliscience101