

FPGA as a multidisciplinary tool for scientific research and industry

a practical example

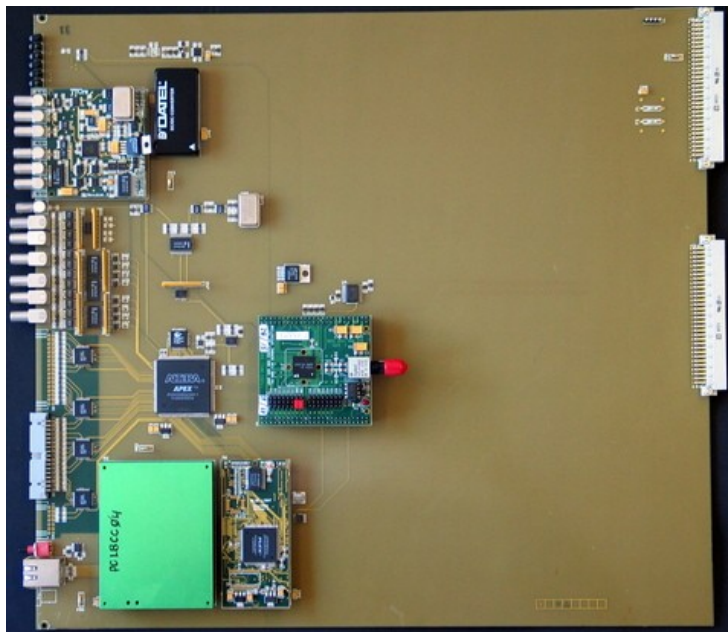
Andrea Borga

digital design engineer and co-founder

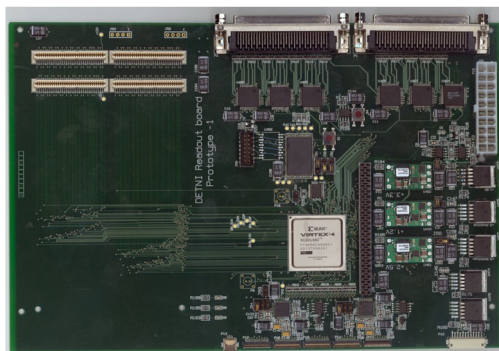
- About myself
- Setting the scene: FPGA
- Nikhef and its activities
- Sharing development efforts
- Technology challenge forecast
- Open Source initiatives at CERN
- Oliscience in a nutshell
- OpenCores
- Closing thoughts

This is me

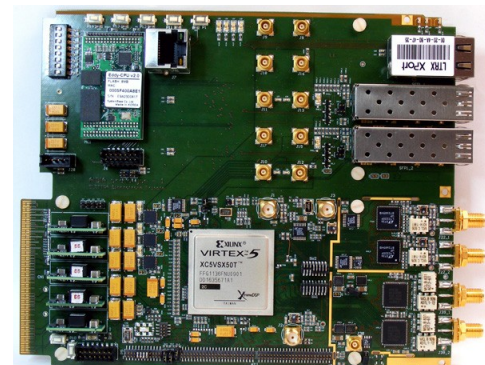
- Digital Designer (aka “the FPGA guy”) specialized in DAQ



CERN – LHCb (2004)



FZ-Juelich – DETNI (2007)

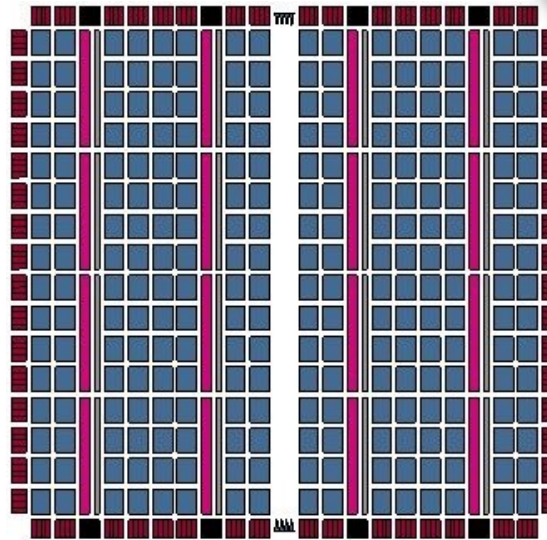
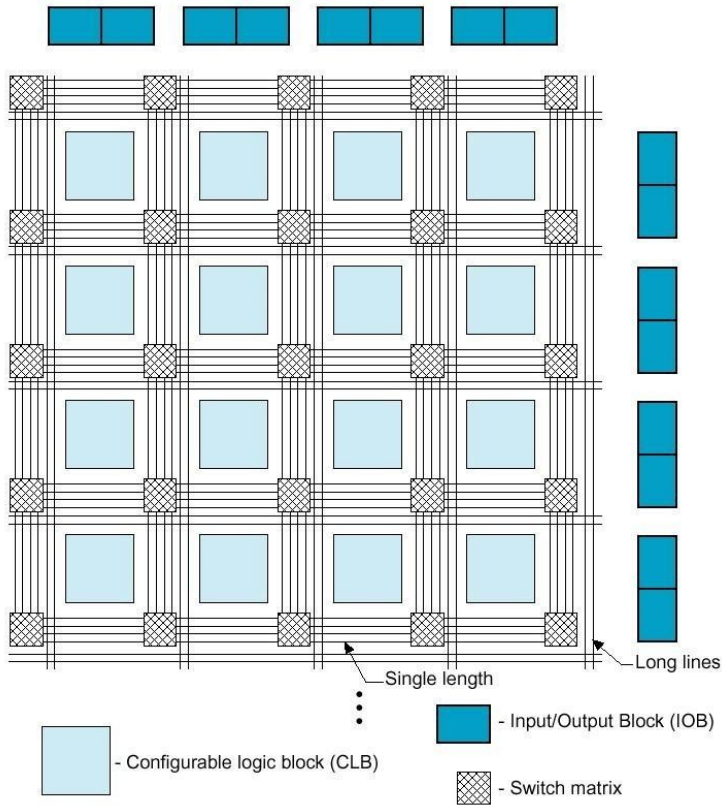


Elettra – FERMI@Elettra (2011)



Nikhef – ATLAS (today)

FPGA... nothing else!



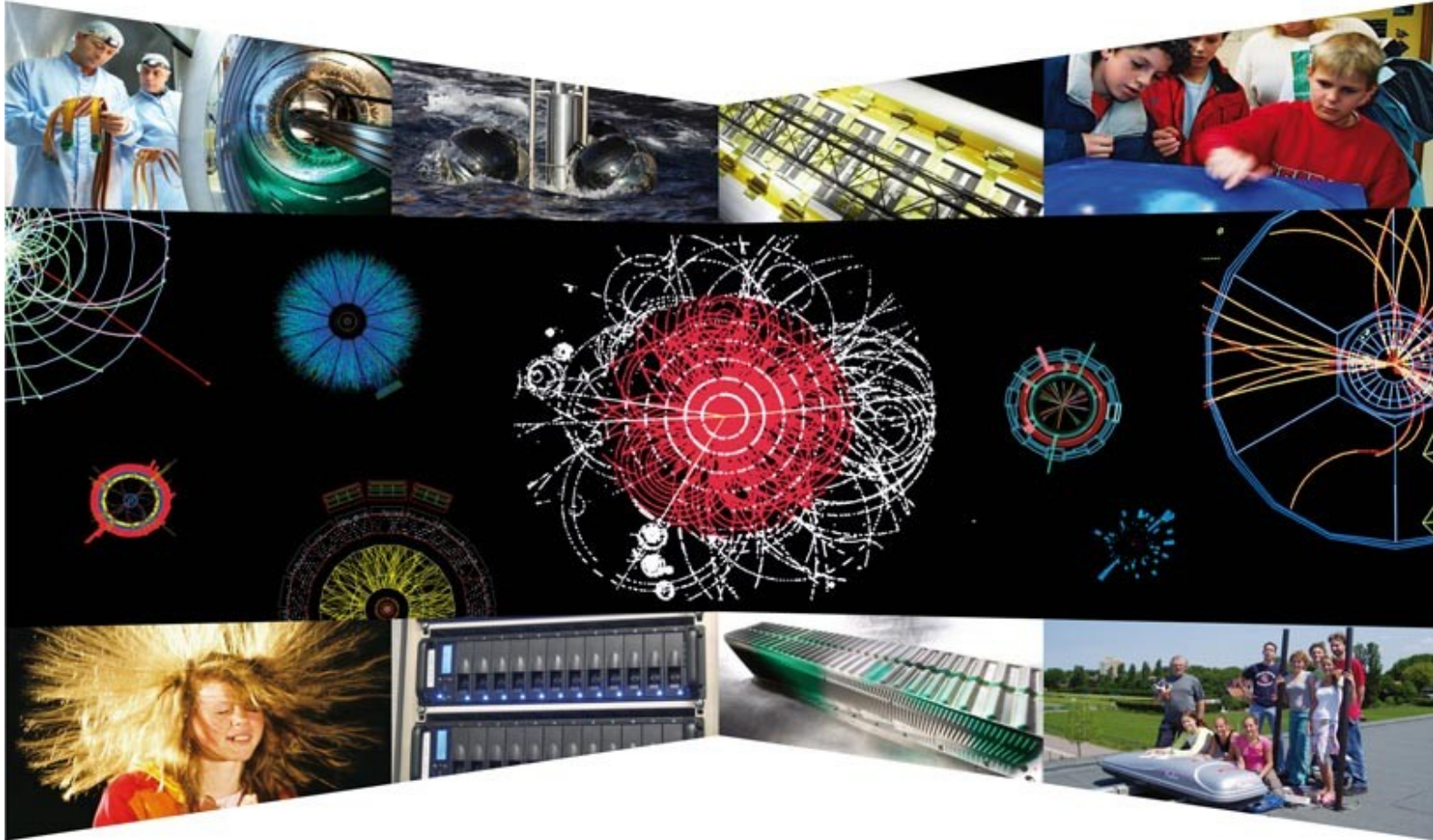
<http://www.xilinx.com>

<http://www.altera.com>

Filling enormous FPGA



About Nikhef

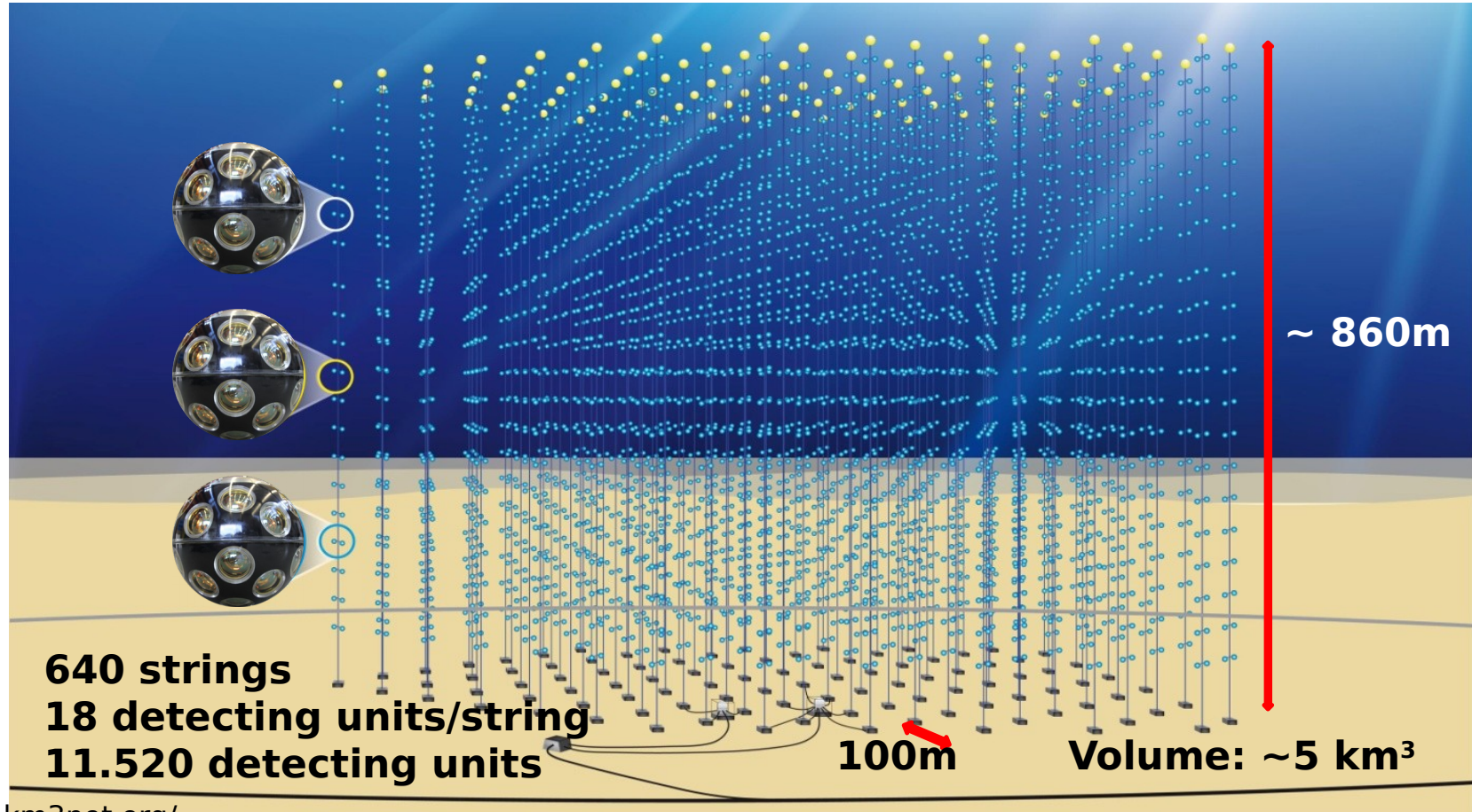


Astroparticle physics



P.C. Budassi, "Observable universe on a log scale" (2016)

Astroparticle physics: Km3Net

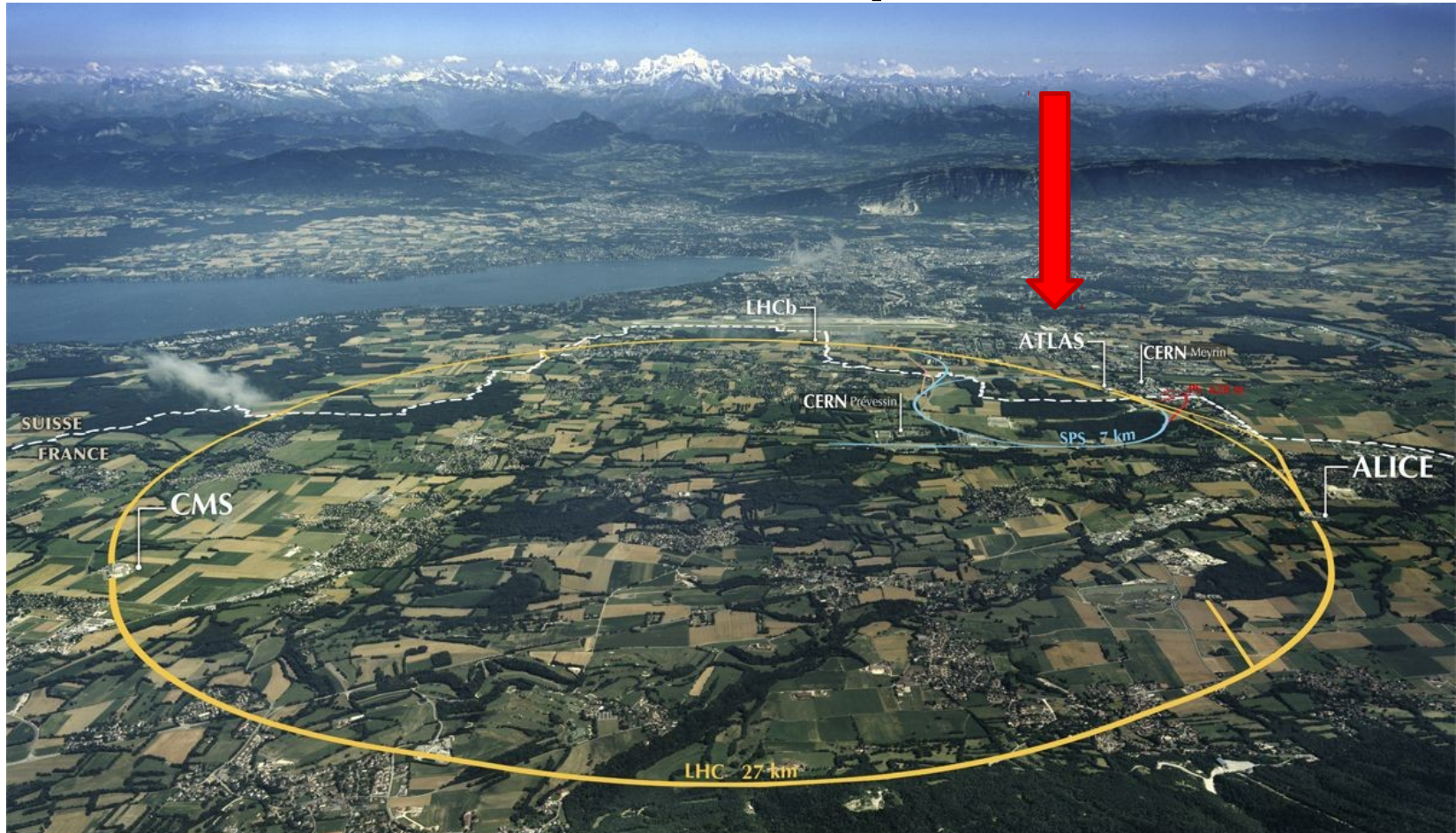


Accelerator physics: CERN LHC

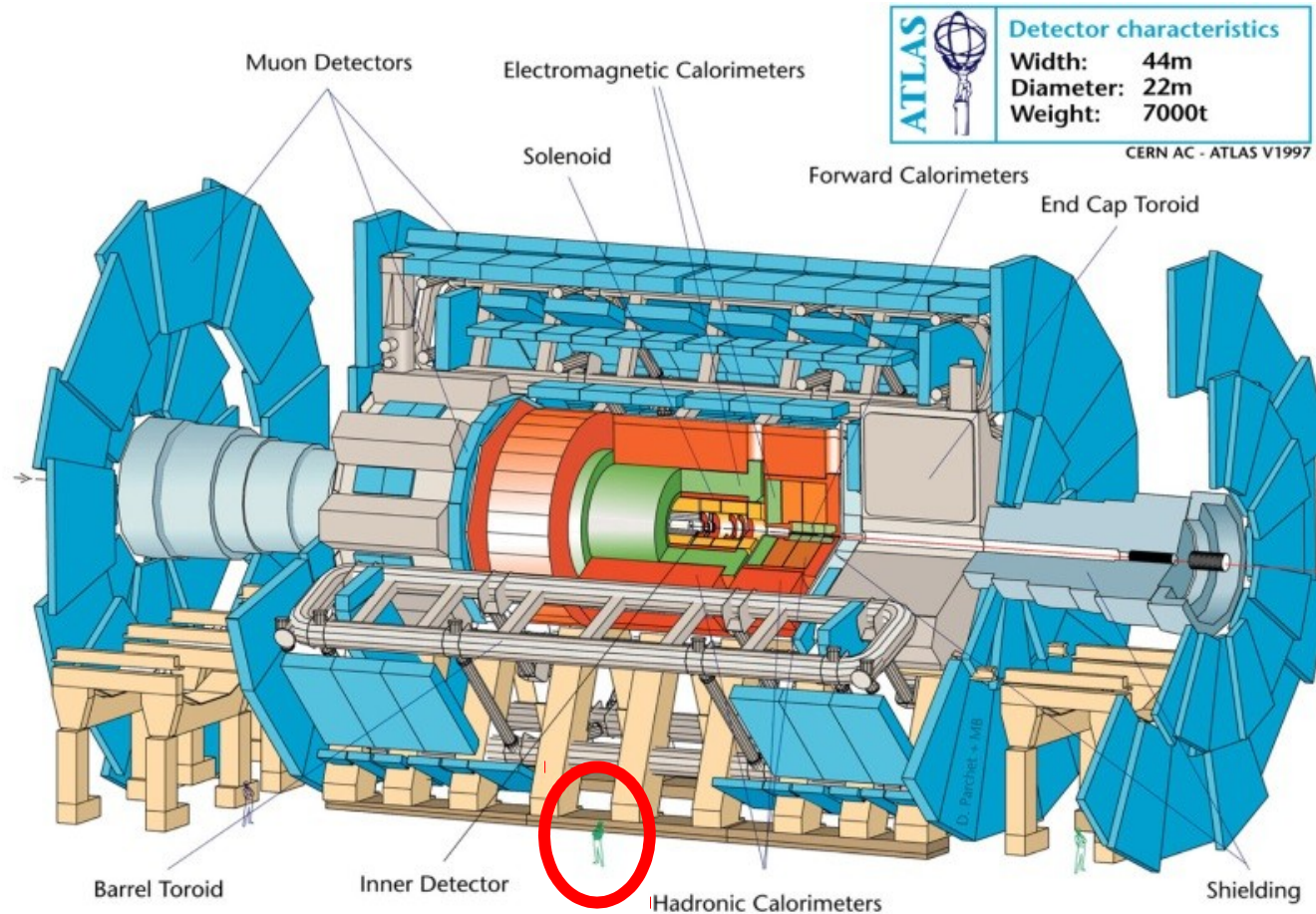


<http://www.cern.ch>

CERN ATLAS Experiment

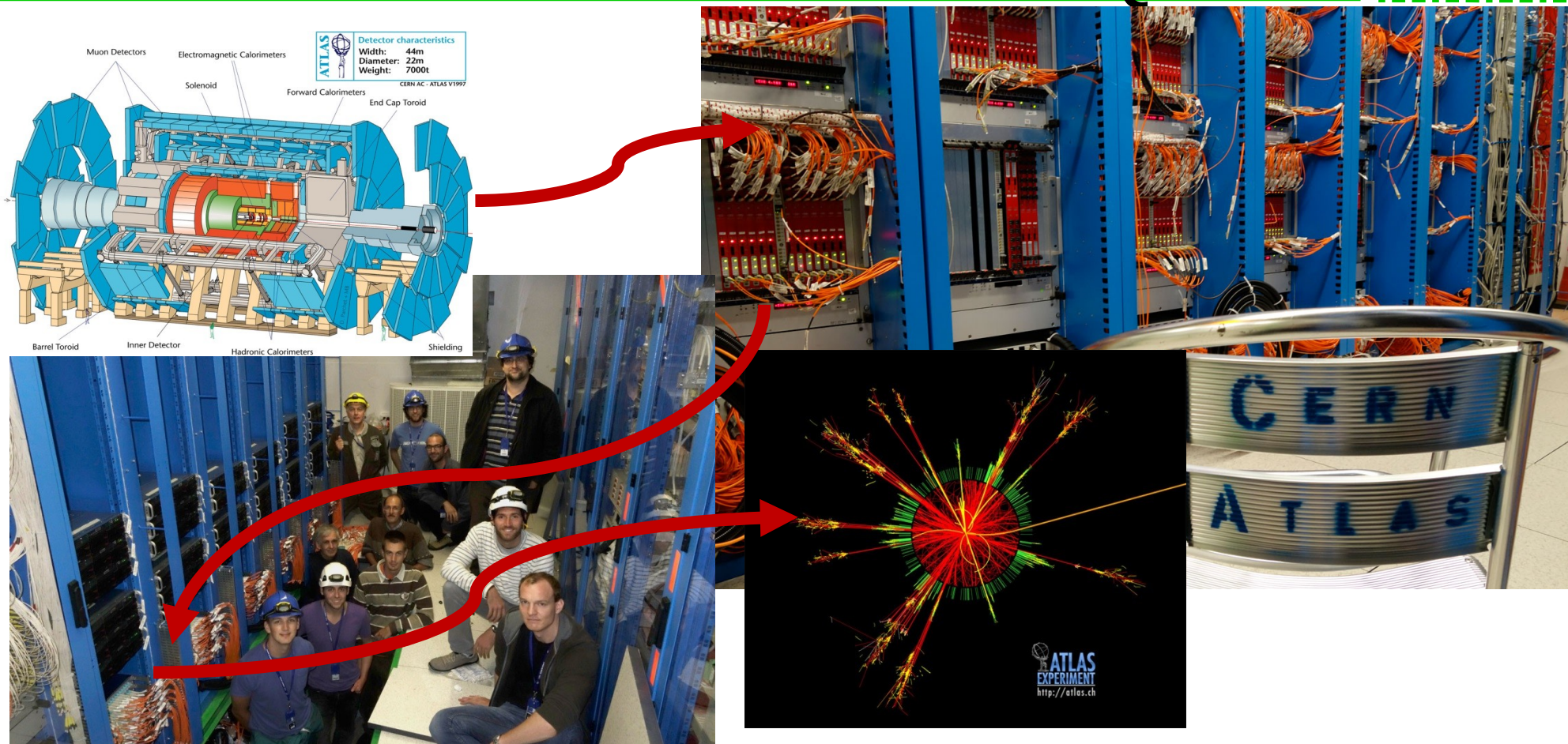


CERN ATLAS detector



<http://atlas.cern>

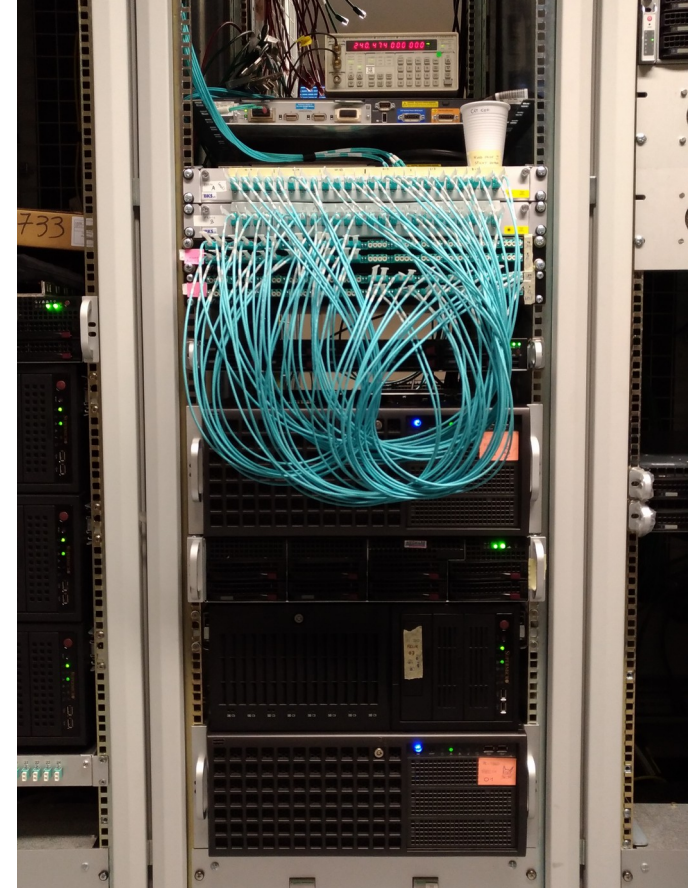
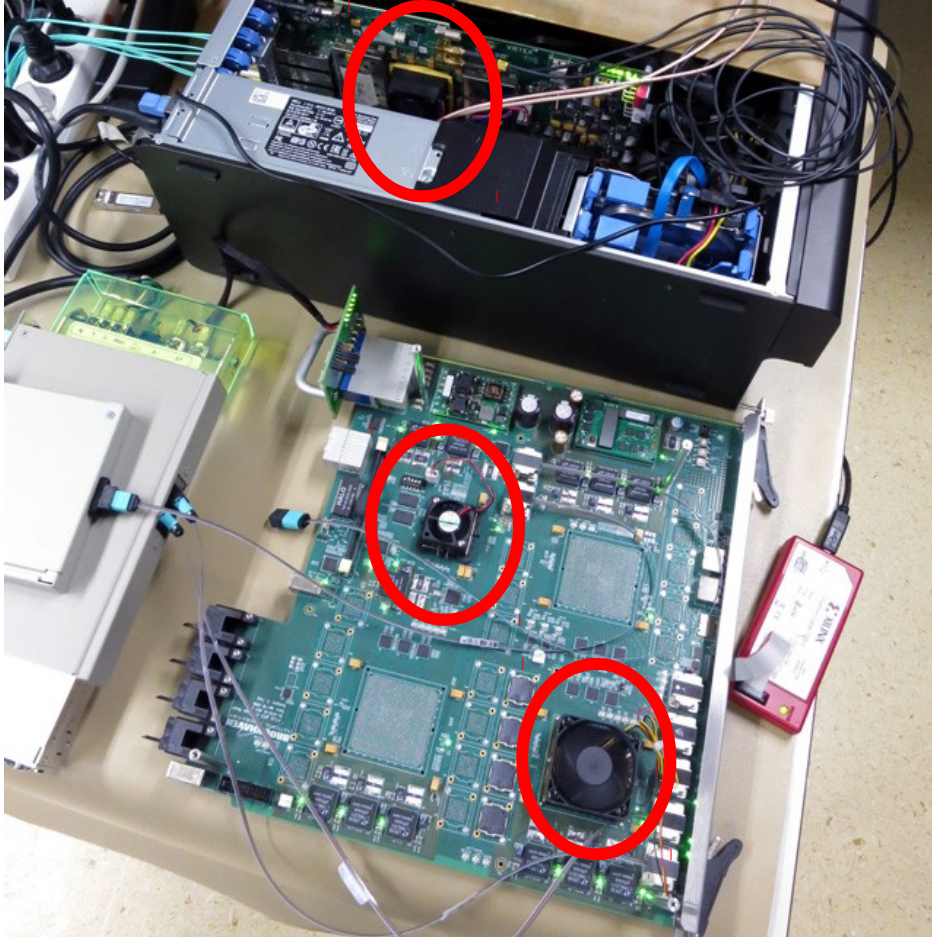
CERN ATLAS DAQ



The need for rad-hard devices.....

- Large experimental physics facilities make use of rad-hard devices (including FPGA) in the following areas:
 - Detector FrontEnds
 - Particle accelerator complexes
- Mostly custom ASICs or Microsemi FPGA
- **This topic not covered in details today...**

FPGA in DAQ systems



<https://atlas-project-felix.web.cern.ch/>

andy@oliscience.nl

At the heart of the matter

★ Wupper: PCIe DMA Engine for Xilinx FPGAs :: Overview

Edit pages

Add a block

Define block order

Help

Overview

Hardware details

Software details

Doxygen

News

Downloads

Bugtracker

Details

Name: virtex7_pcie_dma

Created: Dec 18, 2014

Updated: Apr 7, 2018

SVN Updated: Feb 14, 2018

SVN: [Browse](#)

Latest version: [download](#) (might take a bit to start...)

Statistics: [View](#)

[Bugs](#): 7 reported / 6 solved

★ Unstar 8 you like it: star it!

Other project properties EDIT

Category: [System controller](#)

Language: [VHDL](#)

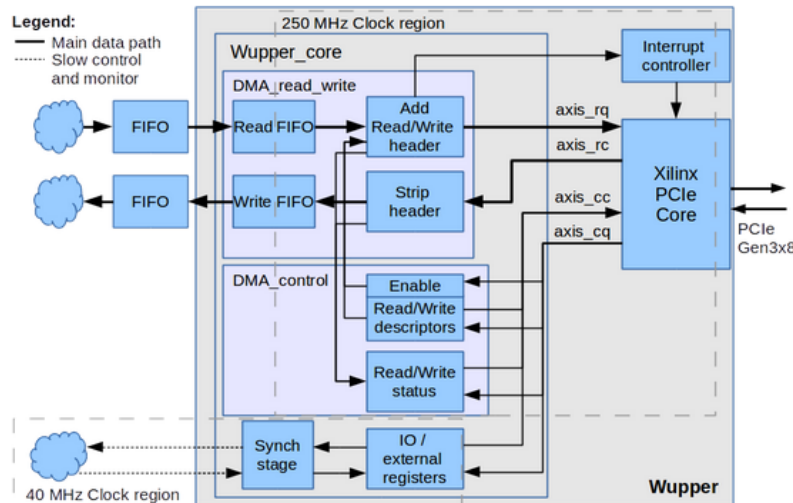
Development status: [Mature](#)

Additional info: [FPGA proven](#), [Specification done](#)

WishBone compliant: No

WishBone version: n/a

License: LGPL



WUPPER



Project maintainers

- [Borga, Andrea](#)
- [Blankers, Roel](#)
- [Schreuder, Frans](#)
- [Kharraz, Oussama](#)
- Add maintainer

Partner team

Nik|hef

✉ nikhef@opencores.org

SpaceWire anyone?

- Browsing OpenCores only...
- https://opencores.org/projects/spacewire_light
- <https://opencores.org/projects/spacewire>
- <https://opencores.org/projects/socwire>
- How many more available “out there”?

FPGA upcoming challenges

- complexity is exponentially growing
- **trust in quality of open source products screams for verification**
 - would you put IP Core “xyz” in space?
- **open standard reference design to compare against?**



Share is the name game

Share... why?

- Get the job done
- Avoid duplication effort
- Seeding of ideas
- Free peer review
- *Sharing in the genes of scientific collaboration*
- A lot of testing done by third parties (**verification**)
- Promote common/good practices (**standardization**)
- Sharing often comes bidirectional



CERN efforts

to share...
or...
to share more!

Javier Serrano from CERN



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OPEN HARDWARE REPOSITORY

[SIGN IN](#) [REGISTER](#)



PROJECTS



FEATURED PROJECTS

CERN BE-CO-HT contribution to KiCad

This project hosts documentation and code to be contributed by CERN's BE-CO-HT section to the KiCad PCB design tool.

[More info at the Wiki page](#)

CERN Open Hardware Licence

A project devoted to developing and discussing the CERN Open Hardware Licence.

[More info at the Wiki page](#)

FMC ADC 100M 14b 4cha

FmcAdc100M14b4cha is a 4 channel 100MSPS 14 bit ADC low pin count FPGA Mezzanine Card (VITA 57). Input ranges: +/-50mV, +/-0.5V, +/-5V. The offset correction by +/- 5V is possible for each gain range. Commercially available.

[More info at the Wiki page...](#)

FMC DEL 1ns 4cha

Welcome

Welcome to the Open Hardware Repository, a place on the web for electronics designers at experimental physics facilities to collaborate on open hardware designs, much in the philosophy of the free software movement. You can get more details about our vision by reading [our manifesto](#).

- Browse the [Projects list](#)
- Read about the [Open Hardware Repository](#)
- Check out the [CERN Open Hardware Licence](#)
- Visit the [Getting Started page](#)

If you need further assistance, or detect a problem with the site, please open a [support ticket](#).

Latest news

OHR Meta Project: "Open Hardware and Collaboration"

as Keynote presentation at PCaPAC.

Added by [Erik van der Bij](#) on [25 Oct 2016 at 10:24](#)

<http://www.ohwr.org>

FPGA in research and industry

andy@oliscience.nl

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HOME PROJECTS LICENSES COMPANIES

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CERN OPEN HARDWARE LICENCE

OVERVIEW

WIKI

ACTIVITY

MAILING LIST

NEWS

DOCUMENTS

CERN Open Hardware Licence - Introduction

Myriam Ayass, legal adviser of the Knowledge and Technology Transfer Group at CERN and author of the CERN OHL:

In the spirit of knowledge sharing and dissemination, the CERN Open Hardware Licence (CERN OHL) governs the use, copying, modification and distribution of hardware design documentation, and the manufacture and distribution of products.

*The CERN-OHL is to hardware what the General Public Licence (GPL) is to software. It defines the conditions under which a licensee will be able to use or modify the licensed material. The concept of 'open-source hardware' or 'open hardware' is not yet as well known or widespread as the free software or open-source software concept. However, it shares the same principles: **anyone should be able to see the source (the design documentation in case of hardware), study it, modify it and share it.***

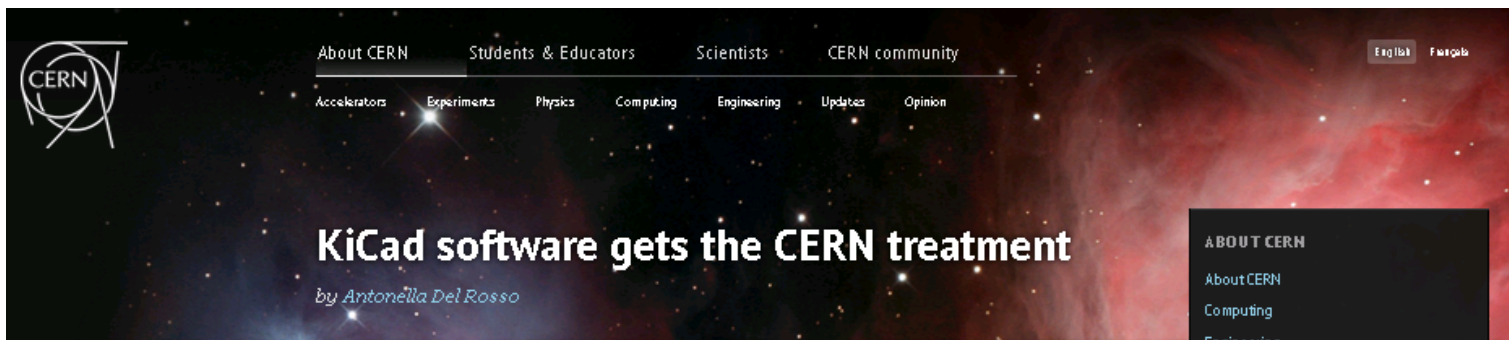
In addition, if modifications are made and distributed, it must be under the same licence conditions – this is the 'persistent' nature of the licence, which ensures that the whole community will continue benefiting from improvements, in the sense that everyone will in turn be able to make modifications to these improvements.

History

Wiki

Start page
Index by title
Index by date

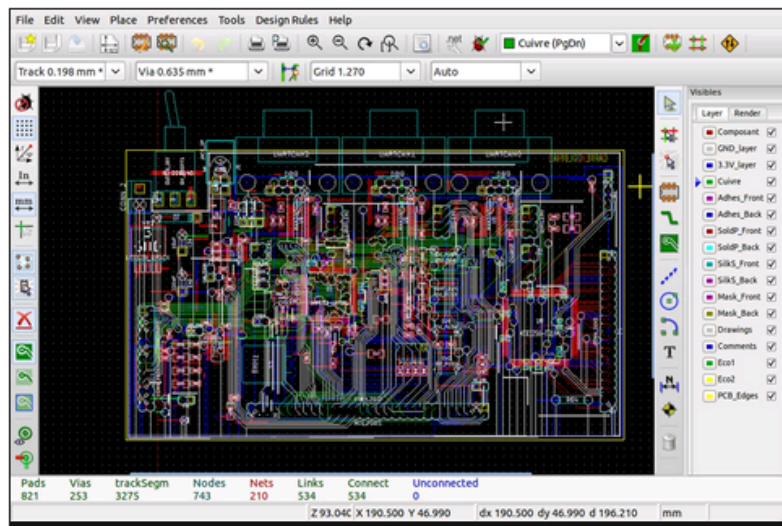
CERN efforts



Posted by [Cian O'Lunaigh](#) on 17 Feb 2015. Last updated 18 Feb 2015, 10.06.

[Voir en français](#)

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[Engineering](#)
[Experiments](#)
[How a detector works](#)

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CERN UPDATES

[A new ring to slow down antimatter](#)
28 Nov 2016
[Meet TIM, the LHC tunnel's robot](#)
25 Nov 2016
[NA64 hunts the mysterious dark photon](#)
25 Nov 2016
[more updates >](#)



oliscience
open logic interconnects science

Oliscience team

- **Alberto Alberton: (sales and marketing)**
 - experienced entrepreneur
 - angel investor in oliscience
- **Leo Davoli: (legal and operations)**
 - professional lawyer
 - angel investor in oliscience
- **Andrea Borga: (CEO and CTO)**
 - seasoned digital design engineer
 - passionate technologist
 - open source enthusiast
 - the geek!



About Oliscience

- Originating from the CERN-BIC at Nikhef

Nikhef

- Coached at Amsterdam Centre for Entrepreneurship

- Based at the Amsterdam Science Park

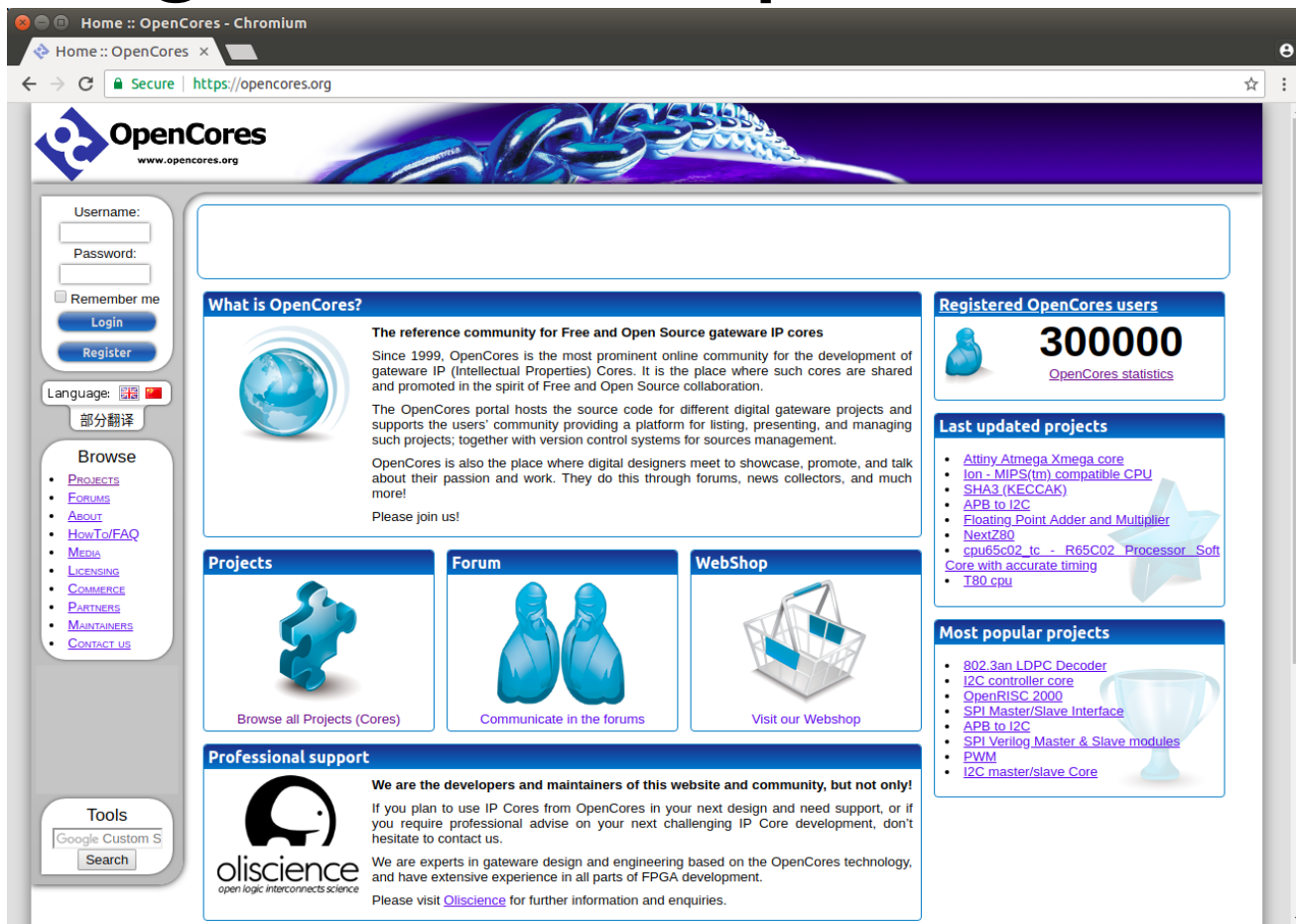
ACE



Oliscience in a nutshell

- Core business: FPGA technology
- Providing consultancy services
- Innovating in the field of FPGA technology
- Driving the OpenCores.org platform:
portal for the exchange of open source IP

The “good old” OpenCores.org



The screenshot shows the OpenCores.org website interface. The header features the OpenCores logo and a navigation bar. The main content area is divided into several sections:

- What is OpenCores?**: A section explaining the community's mission since 1999, providing a platform for sharing and promoting Free and Open Source gateway IP cores.
- Registered OpenCores users**: A section displaying the number of registered users (300000) and a link to OpenCores statistics.
- Last updated projects**: A list of recently updated projects, including Attiny Atmega Xmega core, Ion - MIPS(tm) compatible CPU, SHA3 (KECCAK), APB to I2C, Floating Point Adder and Multiplier, NextZ80, cpu65c02_ic - R65C02 Processor Soft Core with accurate timing, and T80 cpu.
- Most popular projects**: A list of popular projects, including 802.3an LDPC Decoder, I2C controller core, OpenRISC 2000, SPI Master/Slave Interface, APB to I2C, SPI Verilog Master & Slave modules, PWM, and I2C master/slave Core.
- Projects**: A section with a puzzle icon and a link to "Browse all Projects (Cores)".
- Forum**: A section with an icon of two people and a link to "Communicate in the forums".
- WebShop**: A section with a shopping cart icon and a link to "Visit our Webshop".
- Professional support**: A section with the oliscience logo, stating that they are the developers and maintainers of the website and community, and offering professional support for IP Core development.

The left sidebar contains a login/register form, a language selector, and a "Browse" menu with links to Projects, Forums, About, HowTo/FAQ, Media, Licensing, Commerce, Partners, Maintainers, and Contact us. The bottom of the sidebar features a "Tools" section with a Google Custom Search bar.

OpenCores.org in numbers

- Made in Europe!
- Funded in 1999
- Frequented by >300.000 professionals
- Generating ~500.000 views per month
- **Acquired by Oliscience in 2017**
- Steadily increasing activity [up 30% from acquisition]
- Still strong identity, established trademark, consistent community, very specialized

OpenCores.org purpose

- OpenCores brings together Digital Design Engineers
- access to specialized developers
 - OpenCores offers precious insights
 - OpenCores pushes the frontier of possibilities
- **make FPGA and gateware more accessible**
- **push!** ensure that the best IP blocks are used and let them be improved further by the community
- **pull!** encourage more people to add their IP cores

Oliscience goals

- **Stimulate** the community
- **Offer** an “impact metrics” to asses performance
- **Motivate** designers to contribute
- **Offer** a forum for like-minds to meet
- **Promote** best-in-class design practices
- **Provide consultancy services via the portal in the field of gateway design and support**

A call to action to partners

**we develop, drive and promote
the large OpenCores community**

consisting of:

- Research institutions
- Universities
- High-tech corporates

**you access resources on our portal
and contribute fostering common practices**

OpenCores → to the next level.....

- Grow community and increase content
 - many micro processors architectures
 - virtually all standard peripherals
 - a lot of general infrastructure cores
- Increase content **quality and trust**
 - verification, *verification*, verification!
 - standardize methodologies and benchmarks
 - have credited institutions help the process

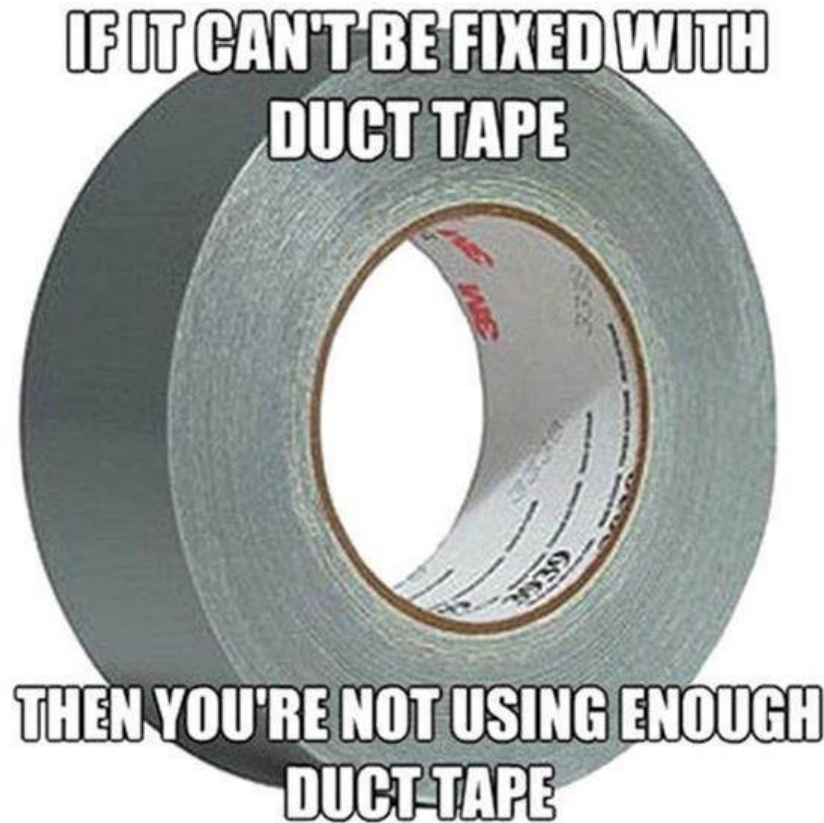


**be the reference market place where
new ideas are exchanged and advanced**

OpenCores → to the next level.....

- Grow con
 - many mic
 - virtually al
 - a lot of ge
- Increase
 - verification
 - standardiz
 - have cred

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Premium partner

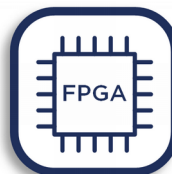
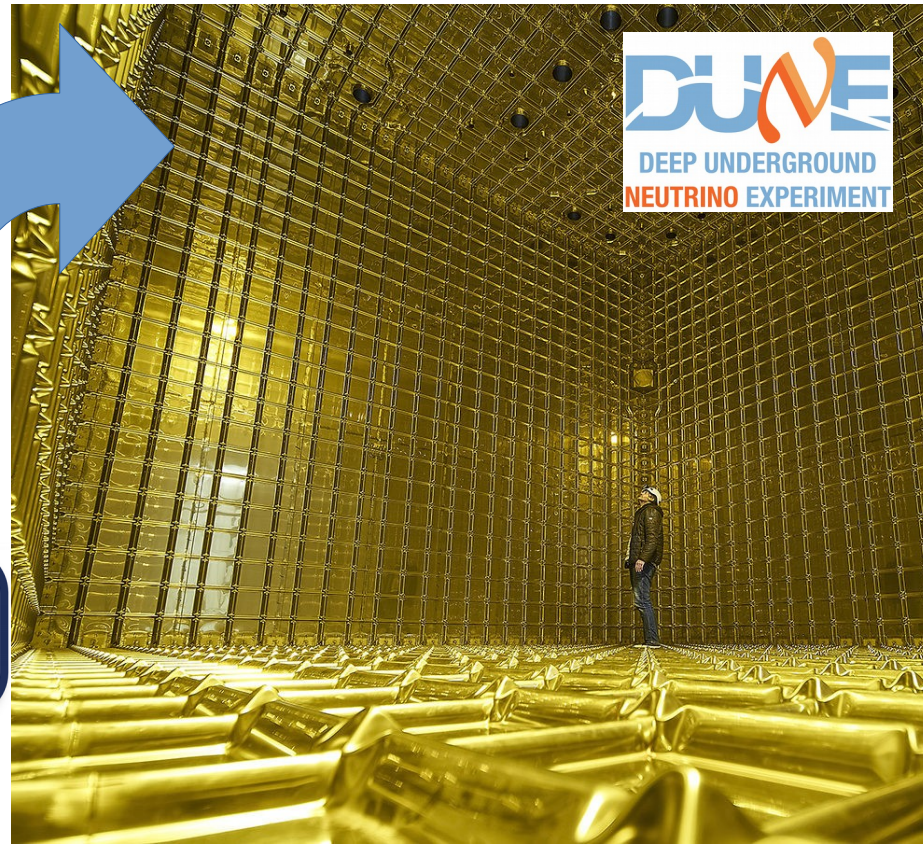
ASTRON

Netherlands Institute for Radio Astronomy

“[...] We are working on the opposite extremes of physics, but we are using the same technology. This collaboration allows us to share ideas and reuse FPGA designs, which will help to speed-up the process of engineering the tools for science.”- *Daniel Van der Schuur*

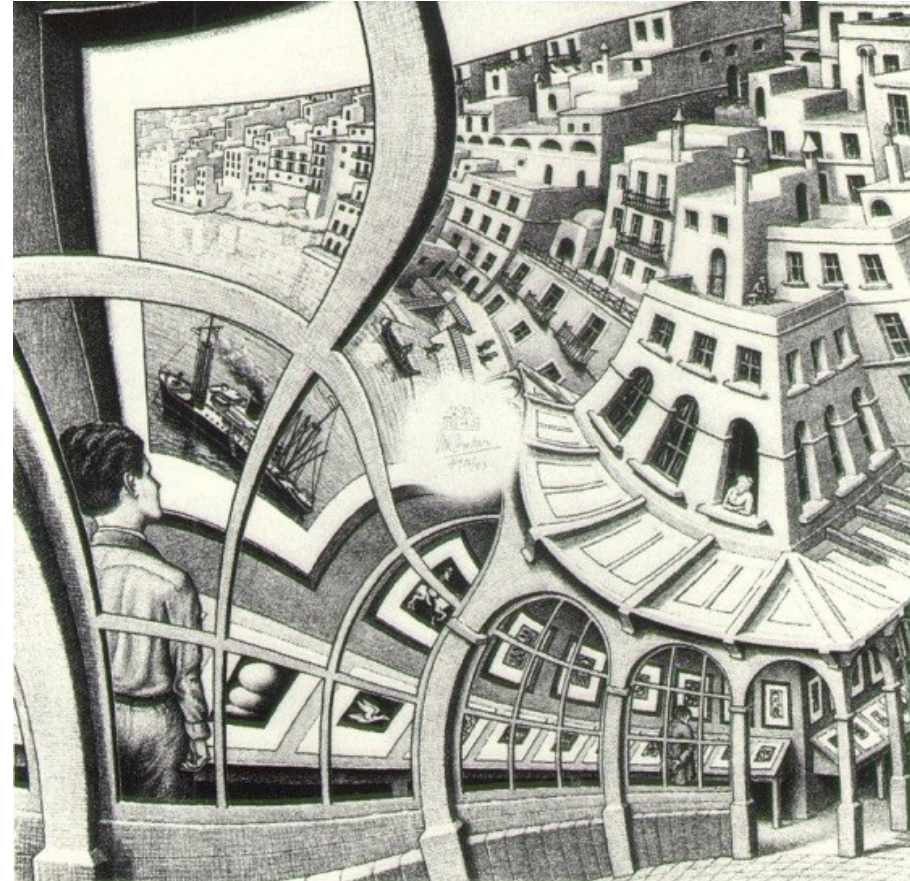


Consultancy customer



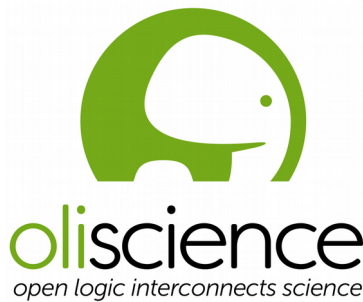
Think different future perspectives

- Overturn common belief
 - open \neq “cheap”
 - look for changes
- Embrace and engage
 - look for alliances
- Cross-contaminate
 - dare to share



M.C. Escher, "Prententoonstelling" (1956)

Thank you



www.opencores.org

www.oliscience.nl

LinkedIn: <https://www.linkedin.com/company/oliscience/>

Twitter: @Oliscience101