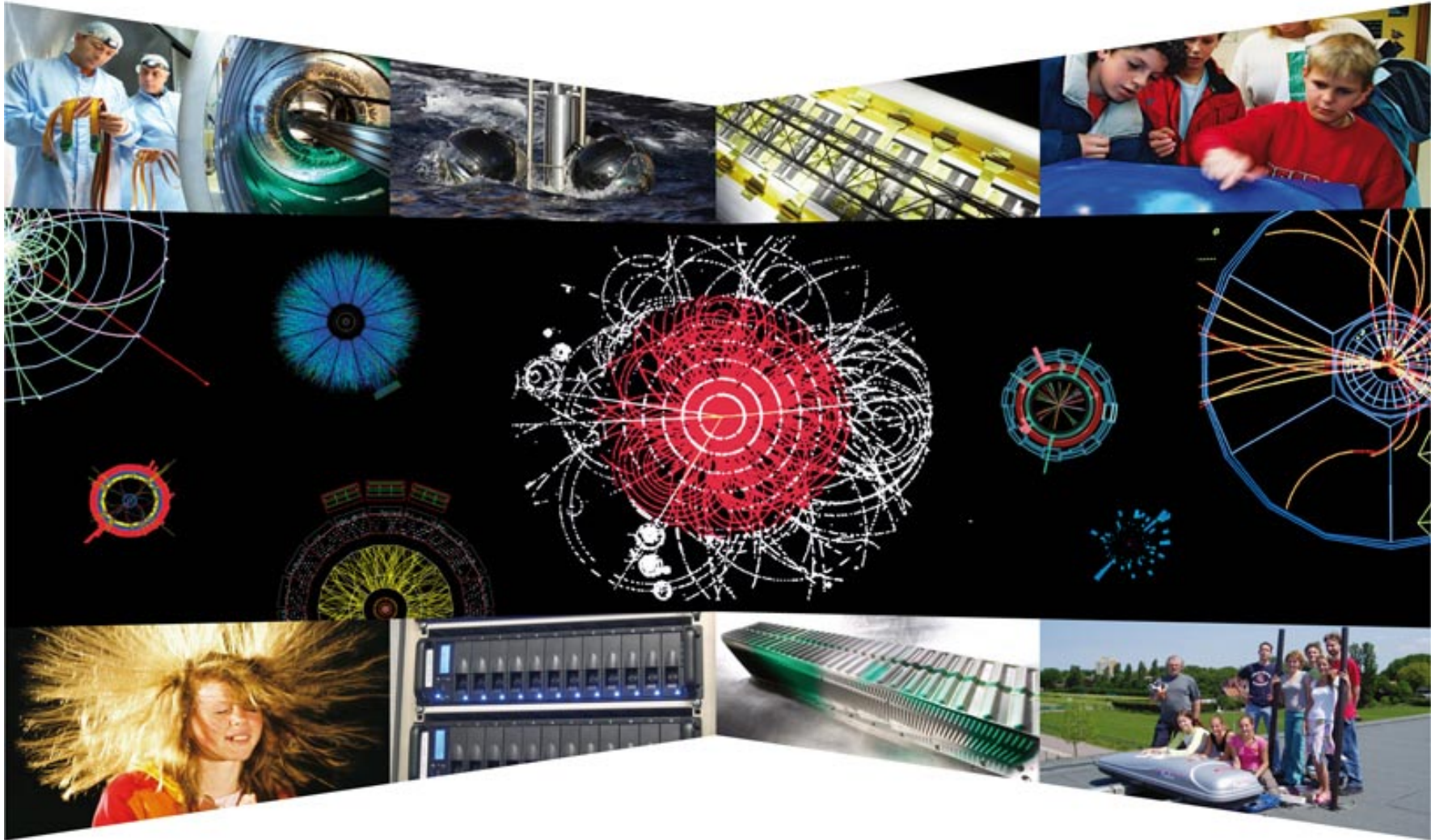


# High Energy Physics and Open Source engineering

accelerate shared knowledge

Andrea Borga  
[andrea.borga@nikhef.nl](mailto:andrea.borga@nikhef.nl)

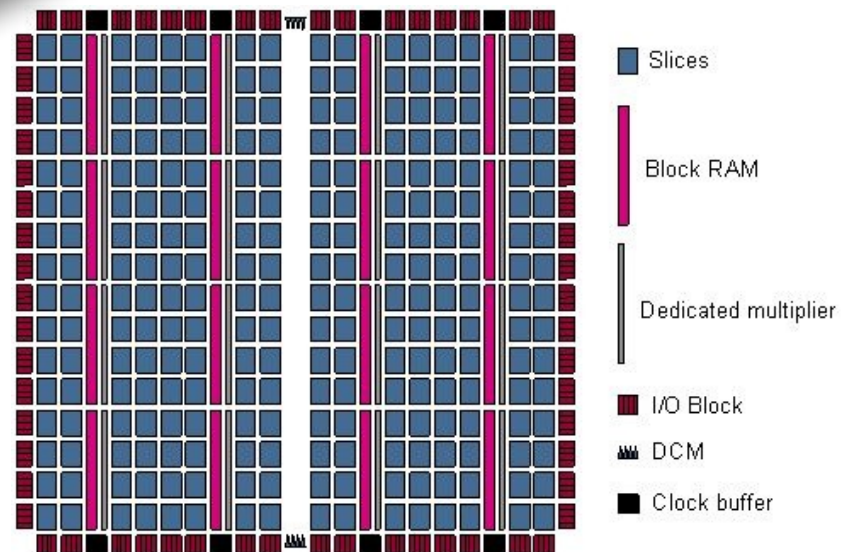
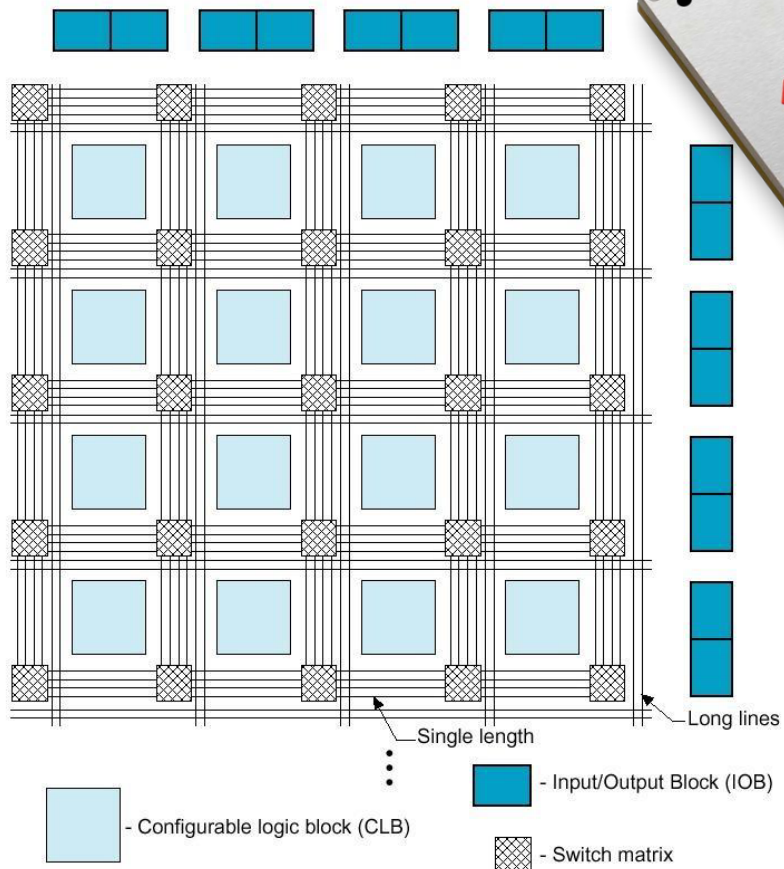
# What is Nikhef?



<http://www.nikhef.nl>

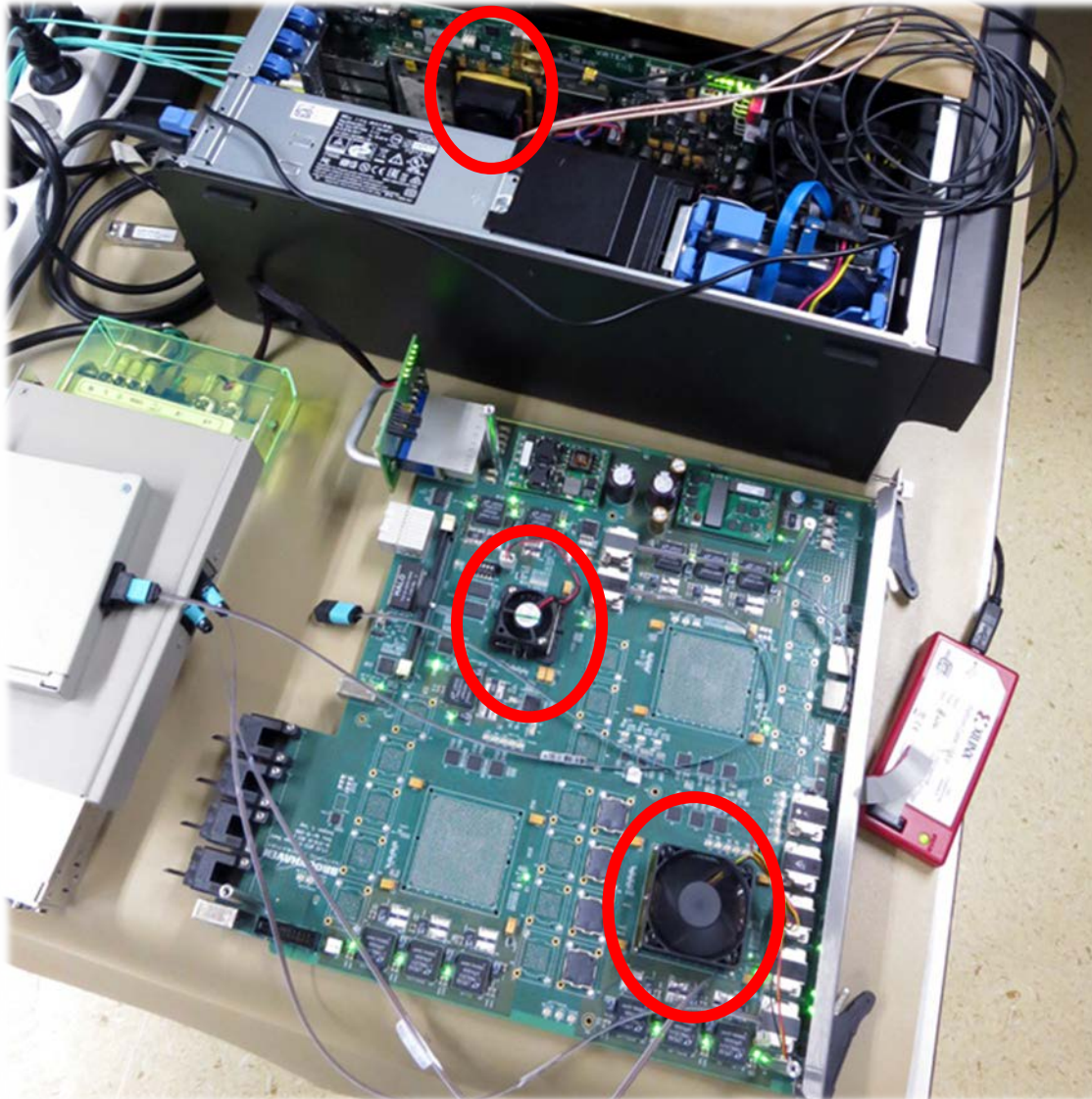


# FPGAs : Field Programmable Gate Arrays



<http://www.xilinx.com>  
<http://www.altera.com>

# FPGAs on Printed Circuit Boards

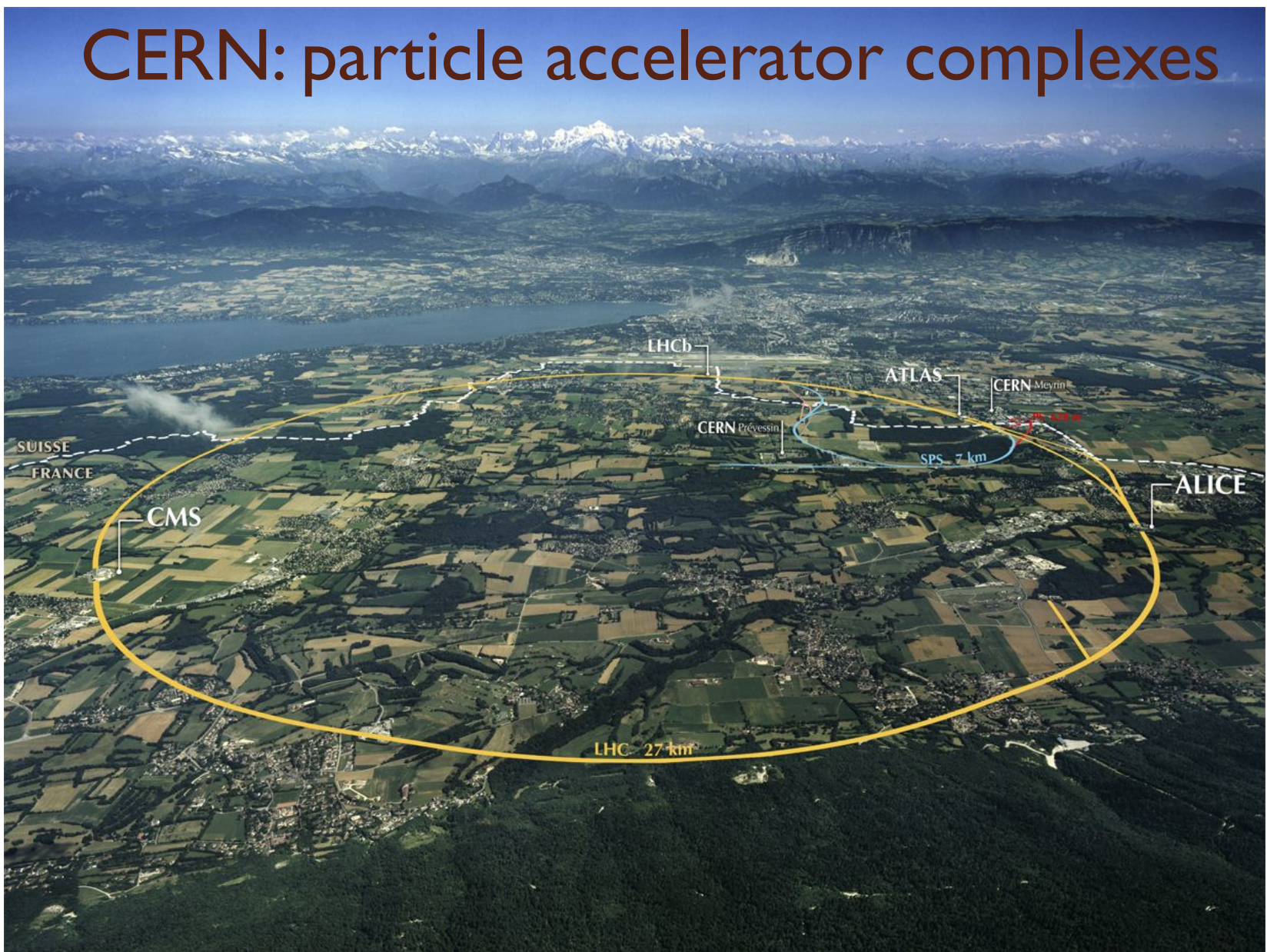


# Filling enormous FPGAs...





# CERN: particle accelerator complexes



<http://www.cern.ch>



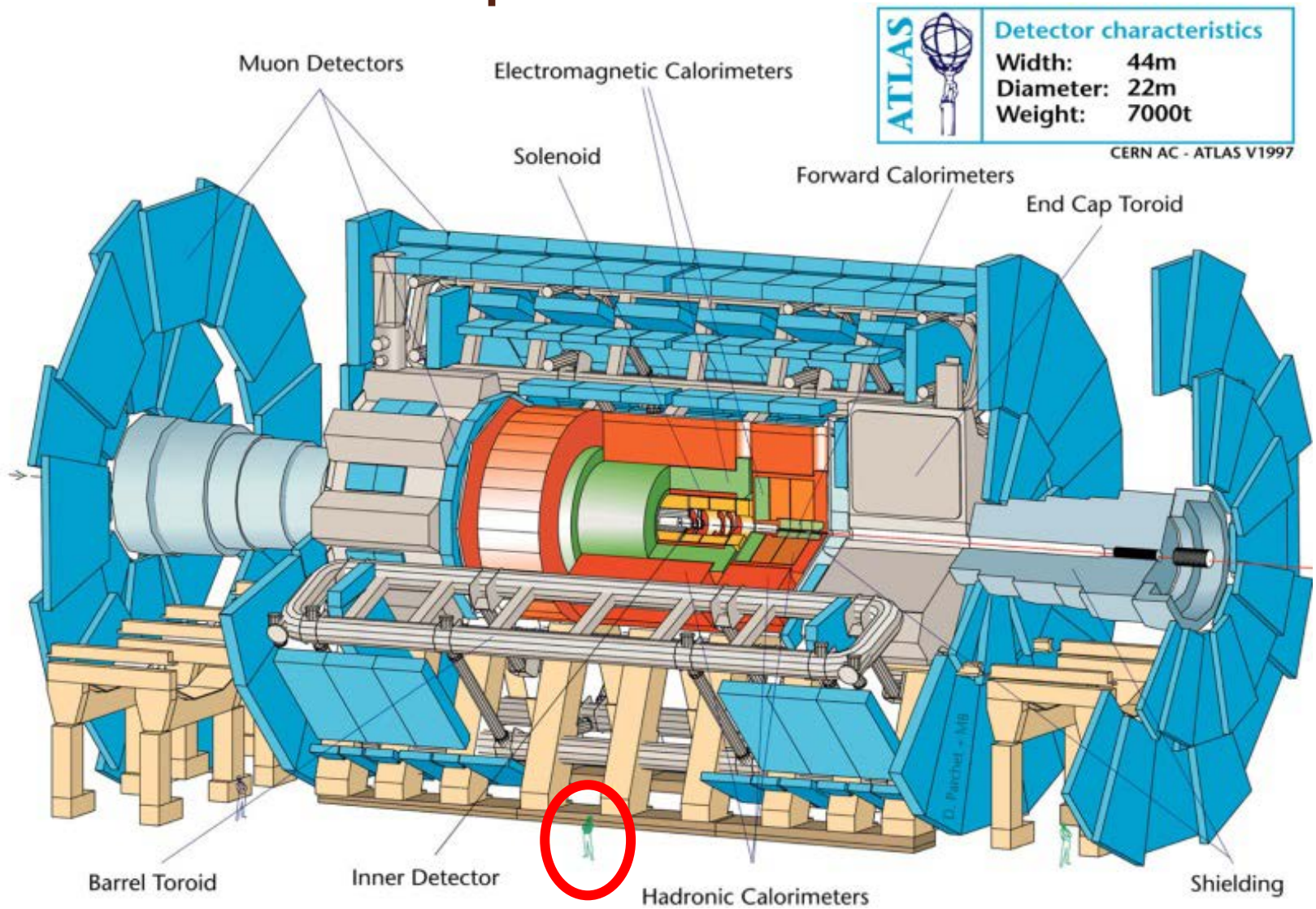
# CERN: particle accelerator complexes



<http://www.cern.ch>



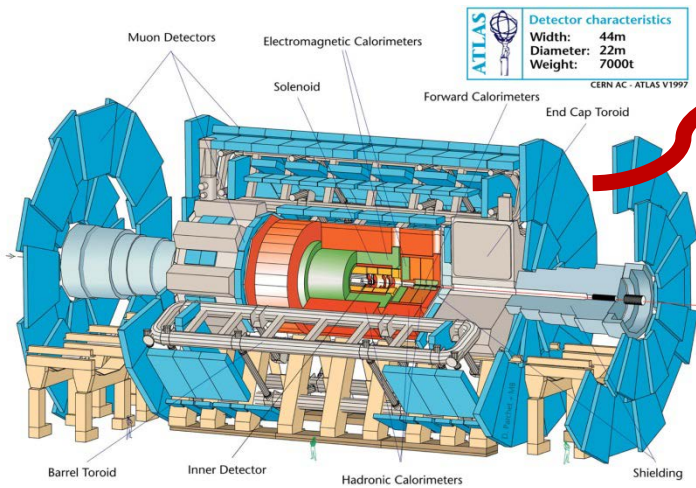
# CERN: particle detectors



<http://atlas.cern>

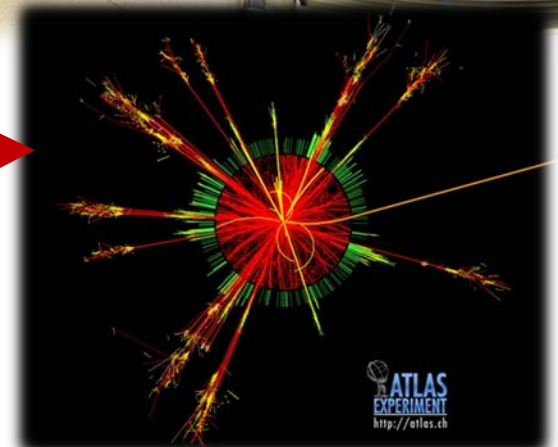
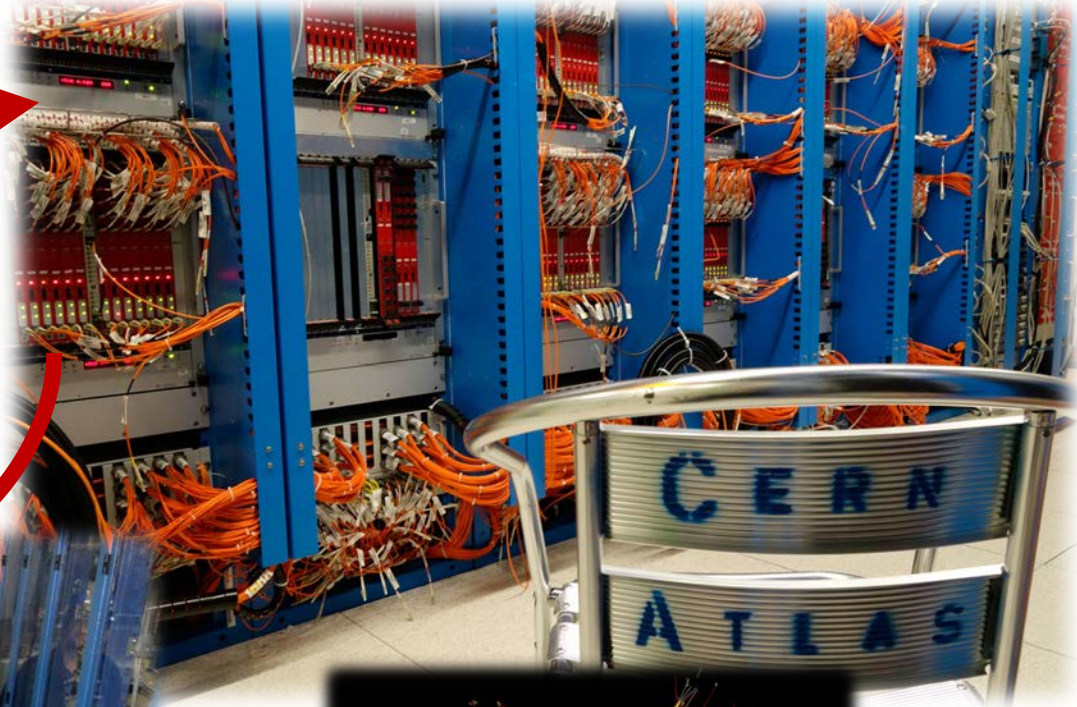


# CERN: particle detectors



ATLAS	Detector characteristics
	Width: 44m Diameter: 22m Weight: 7000t

CERN AC - ATLAS V1997



<http://atlas.cern>



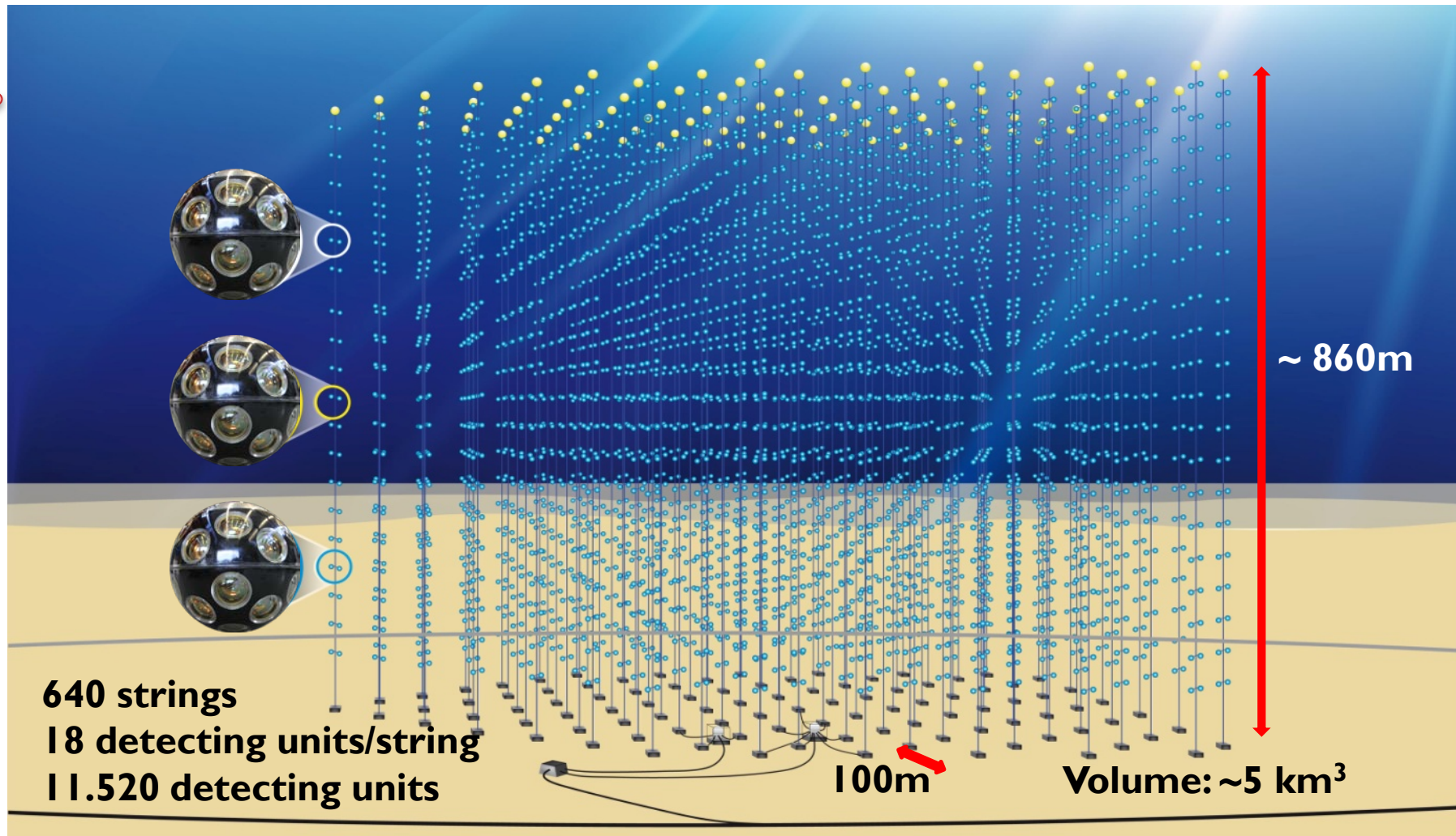
# Astroparticle physics



**P.C. Budassi, "Observable universe on a log scale" (2016)**

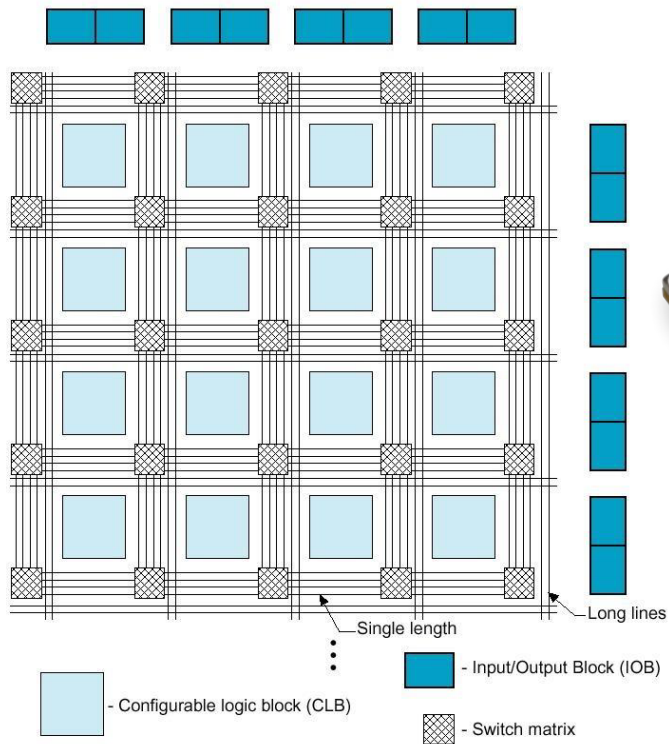


# Astroparticle physics: Km3Net



<https://www.km3net.org/>

# FPGAs: back to the business



- ... One single man cannot fill an FPGA ...
- ... One single group cannot fill an FPGA ...
- The development burden needs to be shared



# Why sharing?

- Get the job done
- Avoid duplication effort
- Seeding of ideas
- Free peer review
- A lot of testing done by third parties
- Sharing often comes bidirectional
- The sum is more than 1





# CERN Open Hardware Repository



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## OPEN HARDWARE REPOSITORY

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### PROJECTS



### FEATURED PROJECTS

#### CERN BE-CO-HT contribution to KiCad

This project hosts documentation and code to be contributed by CERN's BE-CO-HT section to the KiCad PCB design tool.

[More info at the Wiki page](#)

#### CERN Open Hardware Licence

A project devoted to developing and discussing the CERN Open Hardware Licence.

[More info at the Wiki page](#)

#### FMC ADC 100M 14b 4cha

FmcAdc100M14b4cha is a 4 channel 100MSPS 14 bit ADC low pin count FPGA Mezzanine Card (VITA 57). Input ranges: +/-50mV, +/-0.5V, +/-5V. The offset correction by +/- 5V is possible for each gain range. Commercially available.

[More info at the Wiki page...](#)

#### FMC DEL 1ns 4cha

A fine delay generator in FMC format with 1 input and 4 outputs. The resolution is 1 ns. Commercially available.

[More info at the Wiki page](#)

#### FMC DIO 5ch TTL a

FmcDIO5chTTLa is a 5-bit port digital IO card in FMC form-factor. Each single-bit port can be configured individually as input or output. The I/Os that are on LEMO 00 connectors are TTL compatible.

### Welcome

Welcome to the Open Hardware Repository, a place on the web for electronics designers at experimental physics facilities to collaborate on open hardware designs, much in the philosophy of the free software movement. You can get more details about our vision by reading [our manifesto](#).

- Browse the [Projects list](#)
- Read about the [Open Hardware Repository](#)
- Check out the [CERN Open Hardware Licence](#)
- Visit the [Getting Started page](#)

If you need further assistance, or detect a problem with the site, please open a [support ticket](#).

### Latest news

#### OHR Meta Project: "Open Hardware and Collaboration"

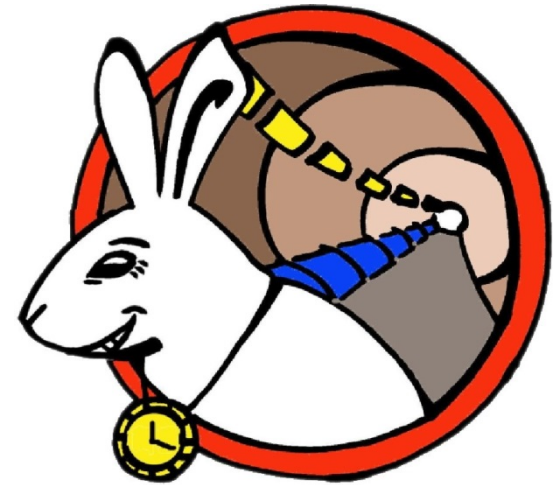
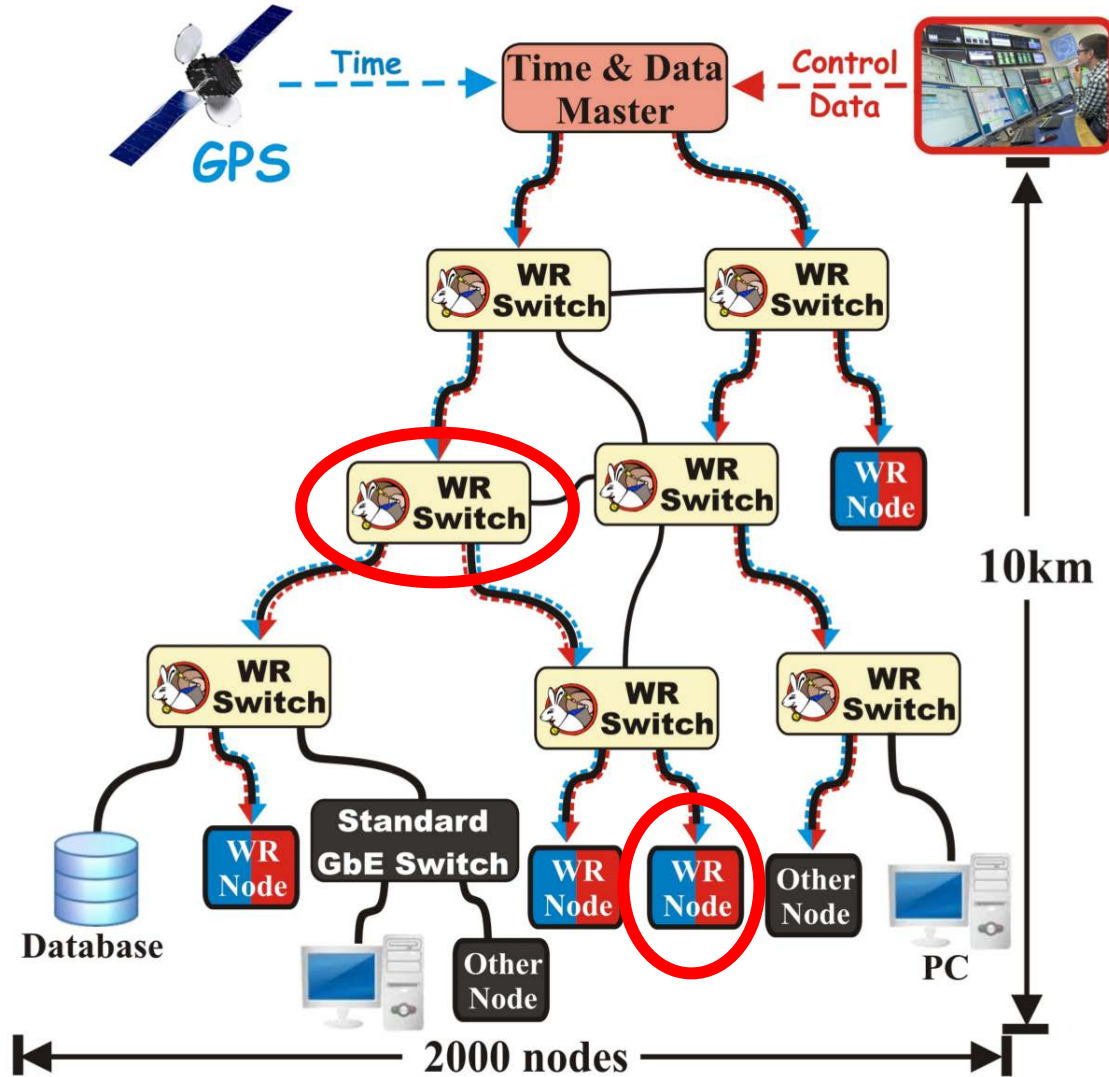
as Keynote presentation at PCaPAC.

Added by [Erik van der Bij](#) on [25 Oct 2016 at 10:24](#)

#### CERN BE-CO-HT contribution to KiCad: a commitment to freedom

In his message [KiCad: A commitment to freedom](#), Javier Serrano thanks the KiCad supporters for their generous donations through the CERN & Society Foundation

# OHWR: the White Rabbit project



Designs can grow  
beyond their  
initial specs



# OHWR: success stories



- Added value to the entire process
- Manufacturing and testing control facilities

<http://www.incaacomputers.com/>


# OpenCores



Welcome back  
Borga, Andrea.

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Language:  

部分翻译

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## Tools

Google™ Custom Search

## What is OpenCores?



### the #1 community within open source hardware IP-cores

OpenCores is the world's largest site/community for development of hardware IP cores as open source.

OpenCores.org host the source code for different digital HW projects (IP-cores, SoC, boards, etc) and support the users with different tools, platforms, forums and other useful information. Please join us!

## Projects



[Browse all Projects \(Cores\)](#)

## Forum



[Communicate in the forums](#)

## WebShop



[Visit our Webshop](#)

## Professional support



### Professional support for OpenCores technology based products.

If you plan to use IPs from OpenCores in your next design and need support, please contact ORSoC AB. They are experts in SoC design based on the OpenCores technology and have extensive experience all parts of FPGA/ASIC development. Please contact [ORSoC](#) for further information.

## Registered OpenCores users



# 267055

[OpenCores statistics](#)

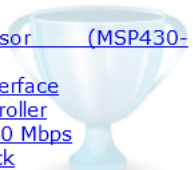
## Last updated projects

- [NEO430 Processor \(MSP430-compatible\)](#)
- [OMS8051 MINI](#)
- [A-Z80 CPU](#)
- [openGFX430](#)
- [turbo 8051](#)
- [FPz8](#)
- [OpenArty](#)
- [mipsr2000](#)



## Most popular projects

- [OpenRISC 1000](#)
- [I2C controller core](#)
- [I2C controller core](#)
- [NEO430 Processor \(MSP430-compatible\)](#)
- [SPI Master/Slave Interface](#)
- [Quad SPI Flash Controller](#)
- [Ethernet MAC 10/100 Mbps](#)
- [1G eth UDP / IP Stack](#)



<http://www.opencores.org>



# OpenCores: PCIe DMA Engine

## PCIe Gen3x8 DMA for virtex7 :: Overview

Edit pages Add a block  
Define block order Help  
Request Implementation Statistics

Overview

Hardware details

Software details

Doxygen

News

Downloads

Bugtracker

### Details





Name: virtex7\_pcie\_dma  
Created: Dec 18, 2014  
Updated: Sep 30, 2016  
SVN Updated: Nov 23, 2016  
SVN: [Browse](#)  
Latest version: [download](#)  
Statistics: [View](#)

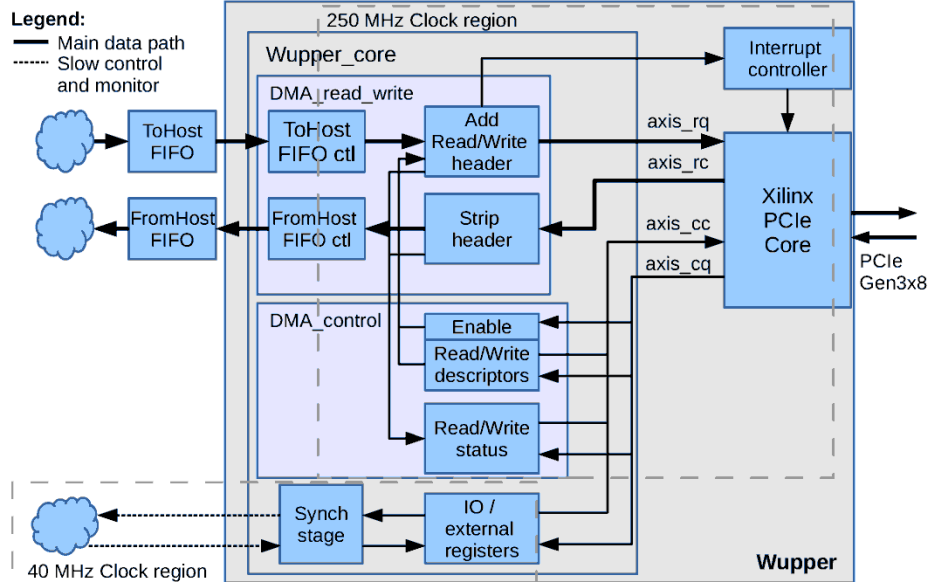
### Other project properties

EDIT

Category: [Communication controller](#)  
Language: [VHDL](#)  
Development status: [Beta](#)  
Additional info: [FPGA proven](#), [Specification done](#)  
WishBone Compliant: No  
License: LGPL

### Project maintainers

- [Borga, Andrea](#) 
- [Schreuder, Frans](#) 
- [Kharraz, Oussama](#) 
-  Add maintainer



WUPPER





**to share...**  
or not to share...

Javier Serrano from CERN



# Challenges: licensing schemes



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## CERN OPEN HARDWARE LICENCE

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## CERN Open Hardware Licence - Introduction

Myriam Ayass, legal adviser of the Knowledge and Technology Transfer Group at CERN and author of the CERN OHL:

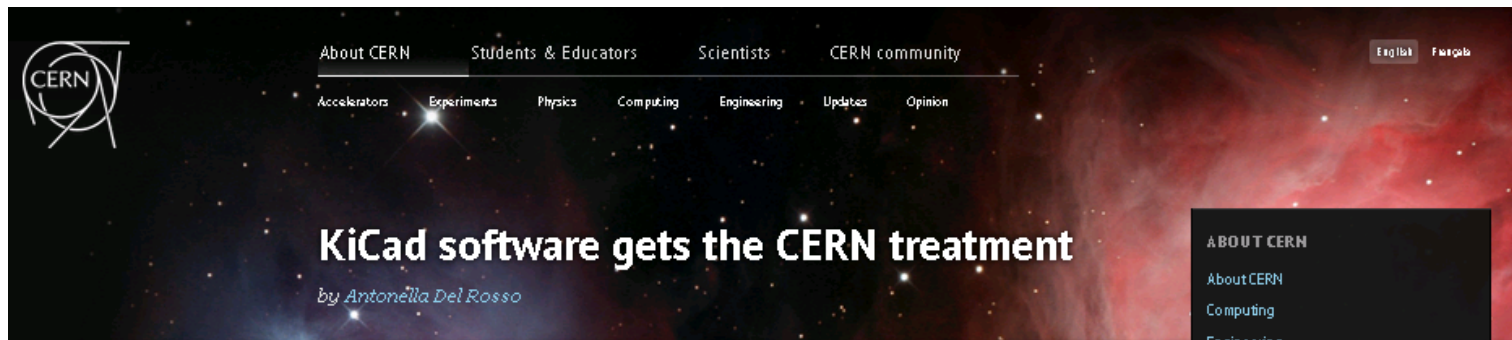
*In the spirit of knowledge sharing and dissemination, the CERN Open Hardware Licence (CERN OHL) governs the use, copying, modification and distribution of hardware design documentation, and the manufacture and distribution of products.*

*The CERN-OHL is to hardware what the General Public Licence (GPL) is to software. It defines the conditions under which a licensee will be able to use or modify the licensed material. The concept of 'open-source hardware' or 'open hardware' is not yet as well known or widespread as the free software or open-source software concept. However, it shares the same principles: **anyone should be able to see the source (the design documentation in case of hardware), study it, modify it and share it.***

*In addition, if modifications are made and distributed, it must be under the same licence conditions – this is the 'persistent' nature of the licence, which ensures that the whole community will continue benefiting from improvements, in the sense that everyone will in turn be able to make modifications to these improvements.*

The CERN Open Hardware Licence was originally written for CERN designs hosted in the Open Hardware Repository. It can also be used by any designer wishing to share design information using a licence compliant with the [OSHWA definition criteria](#). If you would like to contribute to make it better, please subscribe to the [mailing list](#) and submit any issue you may have.

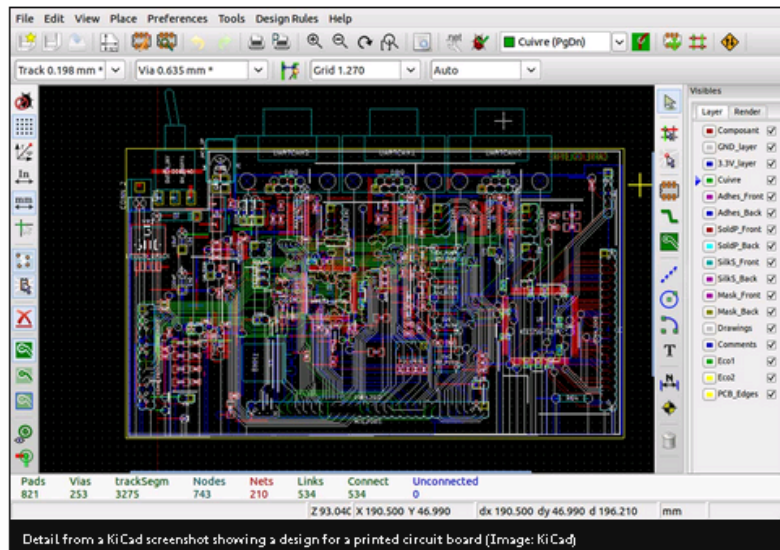
# Challenges: development tools



Posted by [Cian O'Lunaigh](#) on 17 Feb 2015. Last updated 18 Feb 2015, 10:06.

[Voir en français](#)

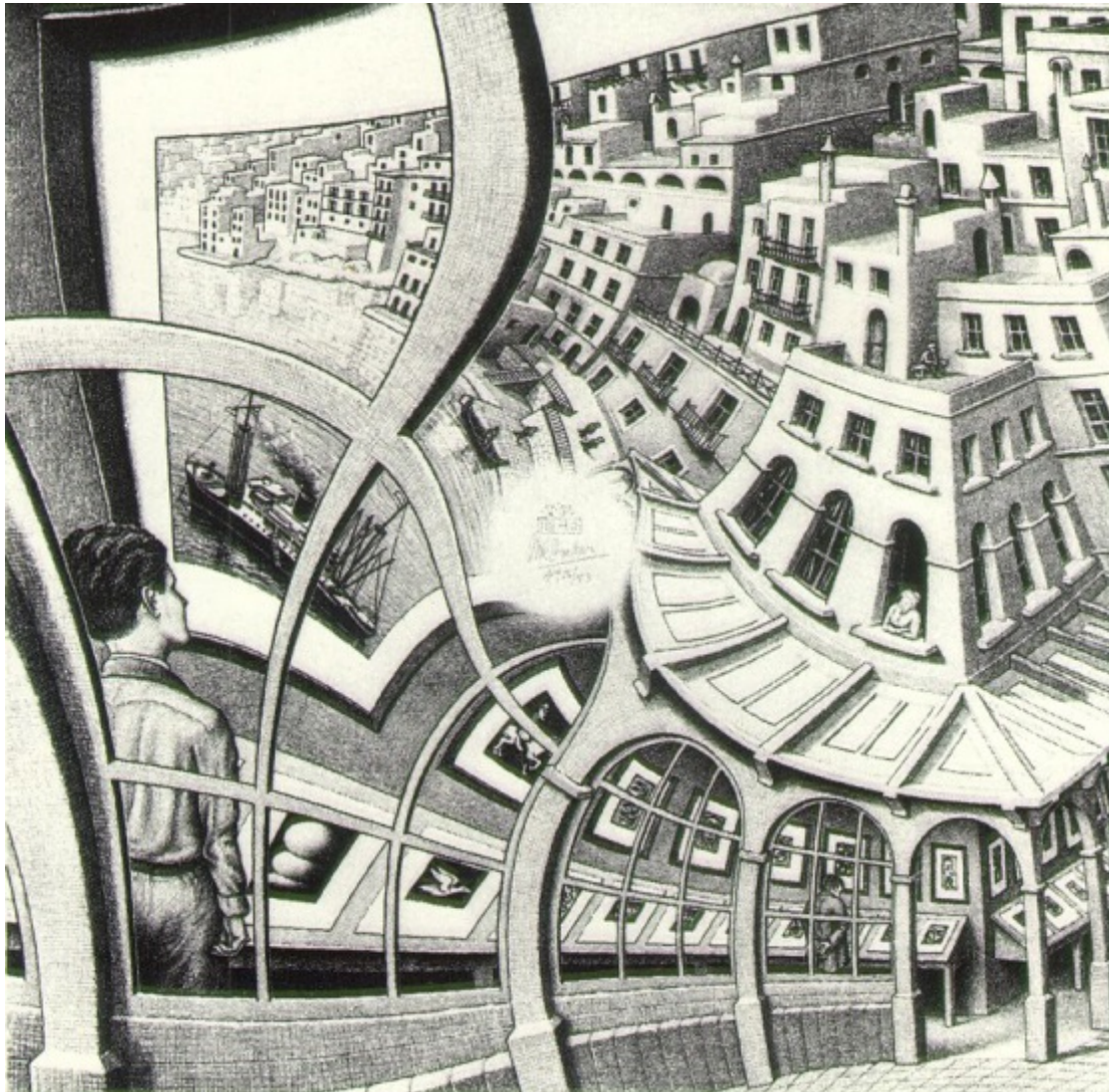
This content is archived on the [CERN Document Server](#)



Printed Circuit Boards (PCB) are the heart of any electronic device, from toasters to smartphones. But so far, the engineers who design the boards often have had no option but to use proprietary tools. That's about to change: CERN experts are adapting the open-source software KiCad to make it an efficient tool for designing open-source hardware. This free software makes it easier for electronics engineers to share their designs.



# think of a different future perspective



M.C. Escher, "Prentententoonstelling" (1956)