

FPGA as a multidisciplinary tool for scientific research and industry

a practical example

Andrea Borga

digital design engineer and co-founder

Outlook

- Oliscience in a nutshell
- Consultancy customers
- Technology challenge forecast
- OpenCores
- OpenCores premium partners
- OpenCores status and plans
- Seeding ideas for better collaboration

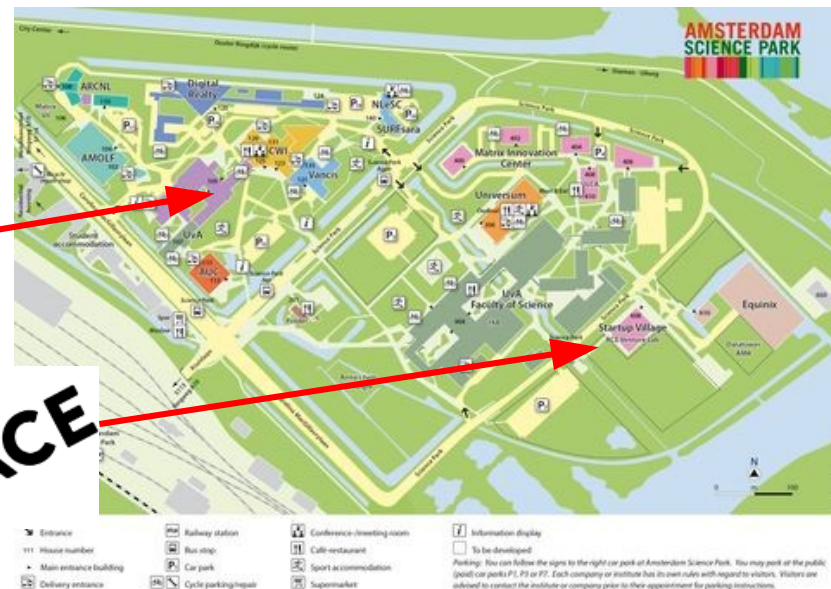
About Oliscience BV

- Originating from the CERN-BIC at Nikhef

Nikhef

- Incubated at Amsterdam
Centre for Entrepreneurship

- Based at the Amsterdam Science Park



Oliscience management team.....

- **Alberto Alberton: (sales and marketing)**
 - experienced entrepreneur
 - angel investor in oliscience
- **Leo Davoli: (legal and operations)**
 - professional lawyer
 - angel investor in oliscience
- **Andrea Borga: (CEO and CTO)**
 - seasoned digital design engineer
 - passionate technologist
 - open source enthusiast
 - the geek!



Oliscience in a nutshell

- Core business: FPGA technology
- Innovating in the field of FPGA
- Providing consultancy services
- Driving the OpenCores.org platform:
community portal for the exchange of Free and
Open Source IP Cores

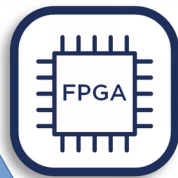
Oliscience consultancy services

- In our **mission**:
“Specialize in the design, streamline, documentation and long term support of gateway Intellectual Property (IP) Cores for FPGA.”
- If digital design is 30% coding + 70% verification and documentation... if anything else we tap into the “remaining” 70!

Consultancy customer

Quantum

Dramatically reduce land seismic acquisition costs with the industry's most efficient sensing system



Quantum pushes the boundaries of seismic sensor networks for on-shore oil & gas exploration and production. Its ultra-low power technology means that each sensor node is significantly smaller, easier to handle, without compromising on sensing performance. This makes the maintenance of large sensor networks simpler, faster and more cost efficient than traditional wired or wireless systems.

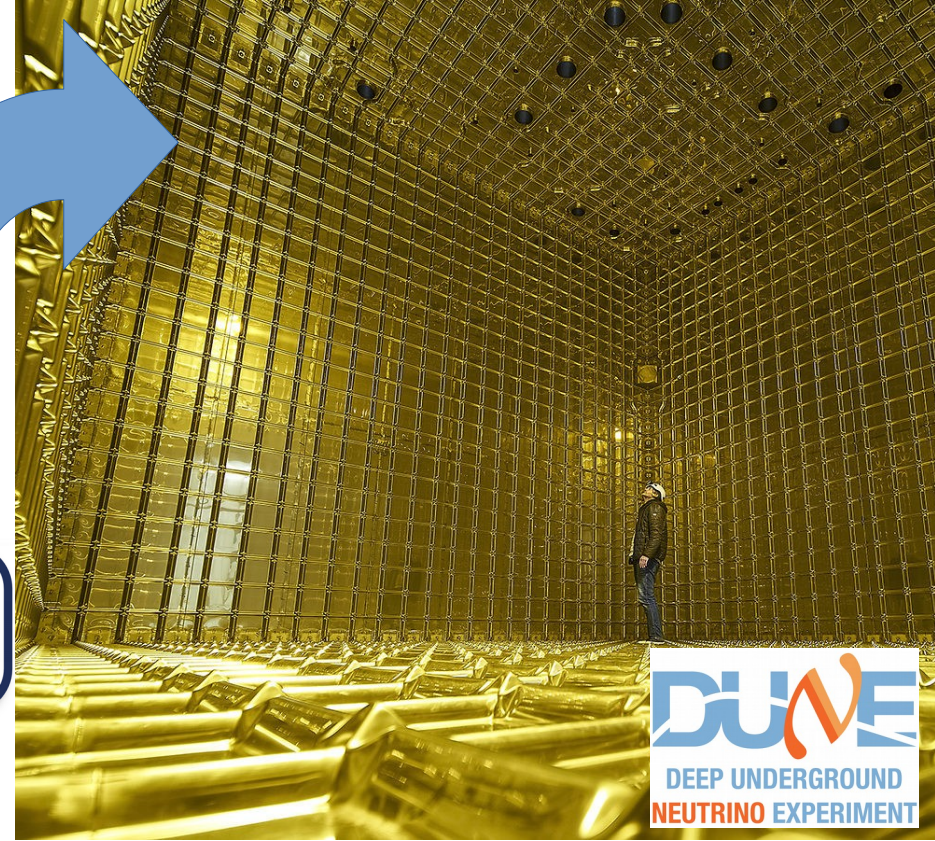
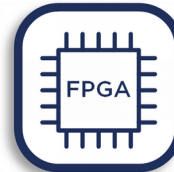
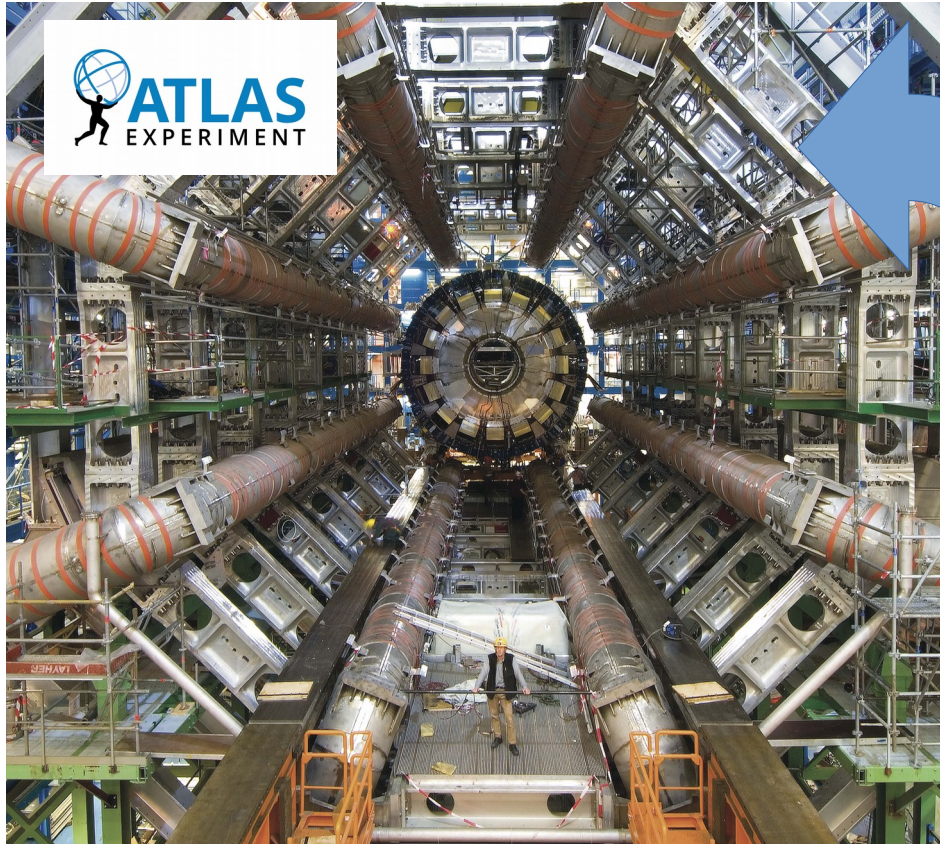
Designed to scale up to million node networks, Quantum allows for higher resolution imaging and more complex survey geometries. It also provides increased topology freedom for various terrains across large survey areas.

Quantum is available with Bluetooth quality control functions for in-field QC and configuration when required. This ensures consistent data quality and eliminates rework.

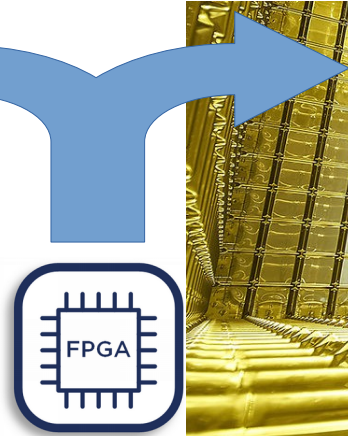
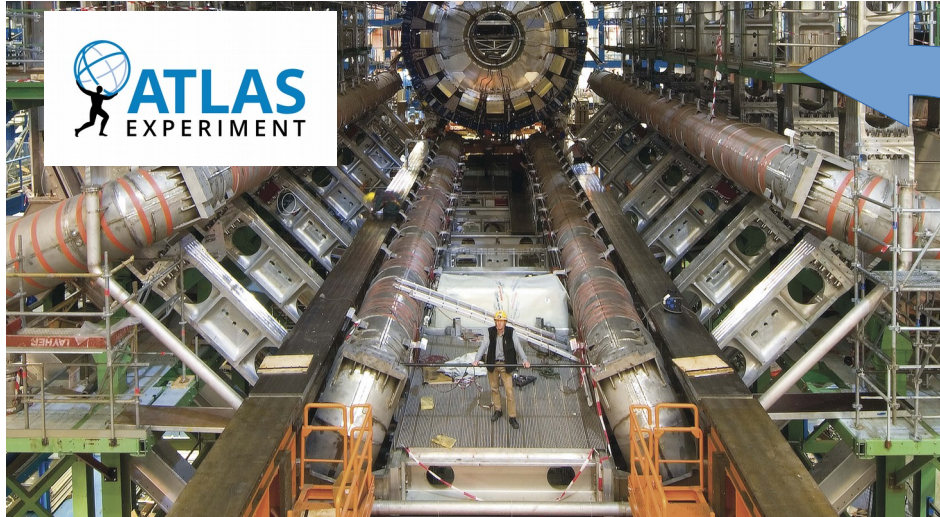
Our systems offer high signal fidelity, autonomous data recording with position and time stamping through GPS functionality, to enable accurate off-line data collection.

- Nasty bug...
- Analysed
- Advised how to pinpoint it
- Iterated
- Fixed the problem
- Advised on general design methodology

Consultancy customer



Crossing the valley of death



- **Valorization...** who's willing to take the risk?
- Proper **technology transfer** is *hard* much harder than hardware... sometimes...

Try this at home?



Toyota Celica ST205 (sixth generation)

FPGA upcoming challenges (1/3).....

- The FPGA world is bustling
 - Nano Xplore → FPGA made EU!
 - Intel PSG → Altera
 - Microchip → Microsemi
 - Canyon Bridge Capital Partners → Lattice
 - Xilinx: The Last of the Mohicans
- The Open Source world is bustling
 - Microsoft → GitHub (7.5 Billions...)
 - IBM → Red Hat (23 Billions...)

FPGA upcoming challenges (2/3).....

- new fields of application are emerging
 - High Performance Computing
 - Hexascale (Heterogeneous) Computing
 - Industry and all the buzz (IoT, AI, ML, ...)
- new design techniques are raising
 - High Level Synthesis vs. OpenCL
 - Python (Migen, MyHDL), Haskell (Clash), P4 (Netcope)
 - Dataflow Engines (Maxeler), Matlab Simulink, ...
- **where to go?**
- **how to get there?**

FPGA upcoming challenges (3/3).....

- complexity is exponentially growing
- **trust in quality of open source products screams for verification**
 - would you put IP Core “xyz” in space?
- **open standard reference design to compare against?**



SpaceWire anyone?

- Browsing OpenCores only...
- https://opencores.org/projects/spacewire_light
- <https://opencores.org/projects/spacewire>
- <https://opencores.org/projects/socwire>
- How many more available “out there”?

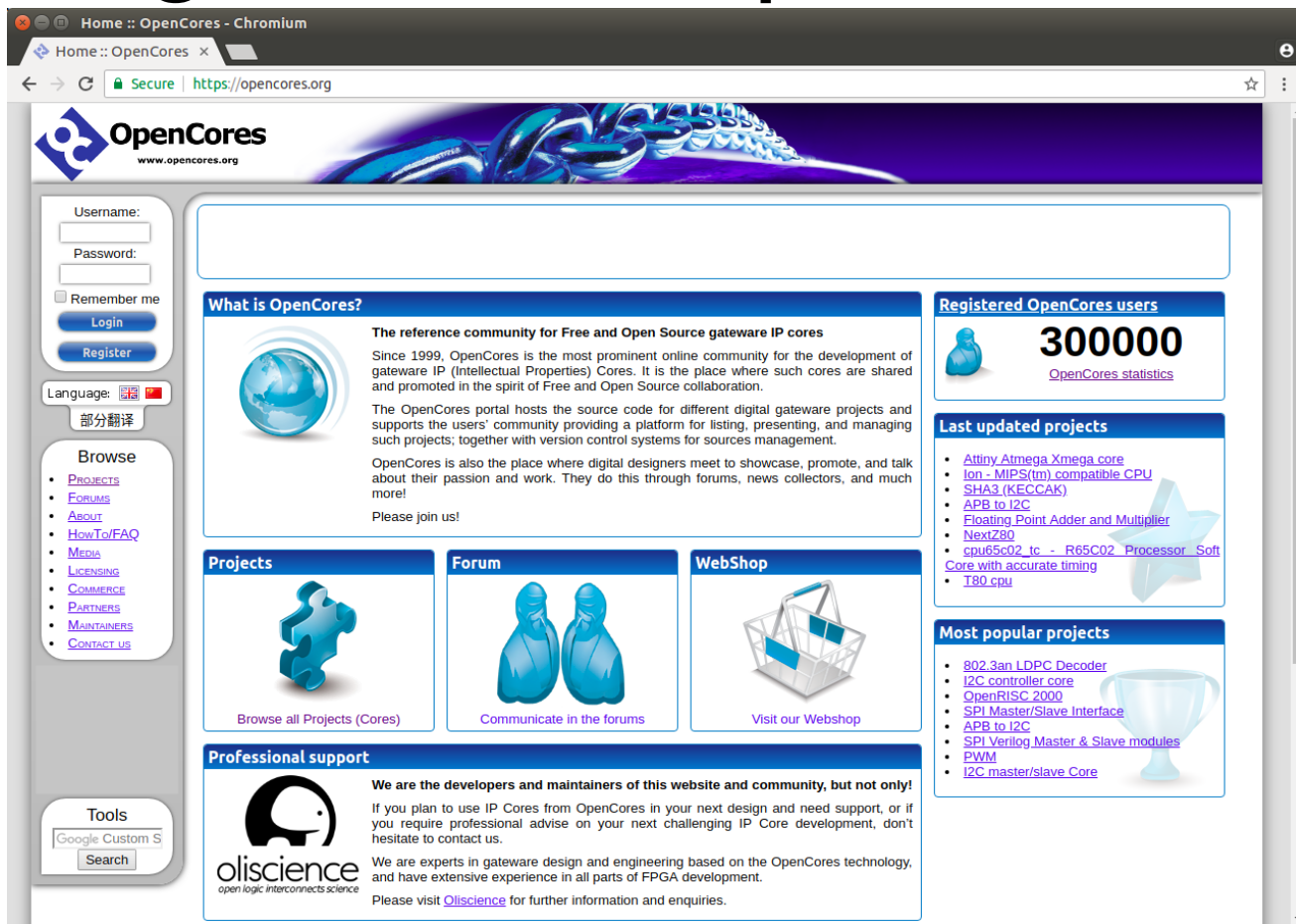
Share is the name game

Share... why?

- Get the job done
- Avoid duplication effort
- Seeding of ideas
- Free peer review
- *Sharing in the genes of scientific collaboration*
- A lot of testing done by third parties (**verification**)
- Promote common/good practices (**standardization**)
- Sharing often comes bidirectional



The “good old” OpenCores.org



The screenshot shows the OpenCores.org website interface. The header features the OpenCores logo and a navigation bar. The main content area is divided into several sections:

- What is OpenCores?**: A section explaining the community's mission since 1999, providing a platform for sharing and managing IP cores.
- Registered OpenCores users**: A section displaying the number of registered users (300000) and a link to OpenCores statistics.
- Last updated projects**: A list of recently updated projects, including Attiny Atmega Xmega core, Ion - MIPS(tm) compatible CPU, SHA3 (KECCAK), APB to I2C, Floating Point Adder and Multiplier, NextZ80, cpu65c02_ic - R65C02 Processor Soft Core with accurate timing, and T80 cpu.
- Most popular projects**: A list of popular projects, including 802.3an LDPC Decoder, I2C controller core, OpenRISC 2000, SPI Master/Slave Interface, APB to I2C, SPI Verilog Master & Slave modules, PWM, and I2C master/slave Core.
- Projects**: A section with a puzzle icon and a link to "Browse all Projects (Cores)".
- Forum**: A section with an icon of two people and a link to "Communicate in the forums".
- WebShop**: A section with a shopping cart icon and a link to "Visit our Webshop".
- Professional support**: A section with the oliscience logo, stating they are developers and maintainers of the website and community, and offering professional support for IP core development.

The left sidebar contains a login/register form, a language selector, and a "Browse" menu with links to Projects, Forums, About, HowTo/FAQ, Media, Licensing, Commerce, Partners, Maintainers, and Contact Us. The bottom of the sidebar features a "Tools" section with a Google Custom Search box.

OpenCores.org in numbers

- Made in Europe!
- Funded in 1999
- Frequented by >300.000 professionals
- Generating ~500.000 views per month
- **Acquired by Oliscience in 2017**
- Still strong identity, established trademark, consistent community, very specialized

OpenCores.org purpose

- OpenCores brings together Digital Design Engineers
- **make FPGA and gateware more accessible**
- **push!** ensure that the best IP Cores are used and let them be improved further by community
- **pull!** encourage more people to add IP Cores

Oliscience goals

- **Stimulate** the community
- **Offer** an “impact metrics” to asses performance
- **Motivate** designers to contribute
- **Steward** a forum for minds-alike to meet
- **Promote** best-in-class design practices
- **Support** our premium partners actively

OpenCores → to the next level.....

- Grow community and increase content
 - many micro processors architectures
 - virtually all standard peripherals
 - a lot of general infrastructure cores
- Increase content **quality and trust**
 - verification, *verification*, verification!
 - standardize methodologies and benchmarks
 - have credited institutions helps the process

**be the reference market place where
new ideas are exchanged and advanced**

A call to action to partners

**we develop, drive and promote
the large OpenCores community**

consisting of:

- Research institutions
- Universities
- High-tech corporates

**you access resources on our portal
and contribute fostering common practices**

Premium partner

ASTRON

Netherlands Institute for Radio Astronomy


“[...] We are working on the opposite extremes of physics, but we are using the same technology. This collaboration allows us to share ideas and reuse FPGA designs, which will help to speed-up the process of engineering the tools for science.”- *Daniel Van der Schuur*



What did we do?



- Prototyped the premium partners section
- Added more prominent display of the affiliated institute on a premium IP Core project
- Created institute@opencores.org alias
- Added a project description parsed from a README.md in the svn repo
- Coded new infrastructure features in nodejs

Premium partners section

**OpenCores**
www.opencores.org

Welcome back
Admin, OpenCores.

[My account](#)
[Logout](#)


Language:  
部分翻译

Browse

- [PROJECTS](#)
- [FORUMS](#)
- [ABOUT](#)
- [HOWTO/FAQ](#)
- [MEDIA](#)
- [LICENSING](#)
- [COMMERCE](#)
- [PARTNERS](#)
- [MAINTAINERS](#)
- [CONTACT US](#)

Admin

- [USERS](#)
- [PROJECTS](#)
- [FORUM](#)
- [ACCOUNT QUE](#)
- [PROJECT QUE](#)
- [NEWS QUE](#)
- [ARTICLE QUE](#)
- [MASS-MAIL](#)
- [NEWS](#)
- [NEWSLETTER](#)
- [NEWSLETTERLIST](#)
- [REDIRECTS](#)
- [SHOP](#)


Netherlands Institute for Radio Astronomy

About
[EDIT](#)
✉ astron@opencores.org

ASTRON is the Netherlands Institute for Radio Astronomy. Its main mission is to make discoveries in radio astronomy happen, via the development of new and innovative technologies, the operation of world-class radio astronomy facilities, and the pursuit of fundamental astronomical research.

Engineers and astronomers at ASTRON have an outstanding international reputation for novel technology development, and fundamental research in galactic and extra-galactic astronomy. To make discoveries in radio astronomy happen, ASTRON invests in modular, reusable and scalable hardware, gateware and software to maintain quality while shortening the time to science.

Projects

- [Library of commonly used components](#)
- [Library of common functions](#)
- [Library of basic components with/for DP streaming interface](#)
- [Library of functions using/for DP streaming interface](#)
- [Generic Data \(width*length\) Repacker](#)

Members

- [van der Schuur, Daniel](#) 🇳🇱
- [Kooistra, Eric](#)

Former members

More prominent presence

★ Wupper: PCIe DMA Engine for Xilinx FPGAs :: Overview

Edit pages

Add a block

Define block order

Help

Overview

Hardware details

Software details

Doxygen

News

Downloads

Bugtracker

WUPPER



Details

Name: virtex7_pcie_dma

Created: Dec 18, 2014

Updated: Apr 7, 2018

SVN Updated: Feb 14, 2018

SVN: [Browse](#)

Latest version: [download](#) (might take a bit to start...)

Statistics: [View](#)

[Bugs](#): 7 reported / 6 solved

★ Unstar 8 you like it: star it!

Other project properties [EDIT](#)

Category: [System controller](#)

Language: [VHDL](#)

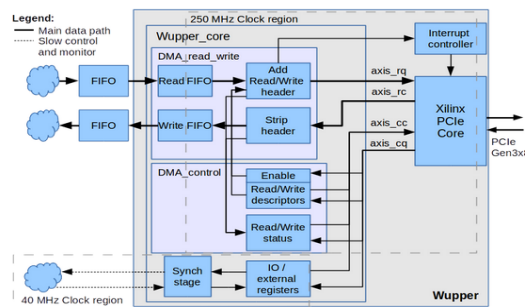
Development status: [Mature](#)

Additional info: [FPGA proven](#), [Specification done](#)






WishBone compliant: No

WishBone version: n/a

License: LGPL



Project maintainers

- [Borga, Andrea](#) 
- [Blankers, Roel](#) 
- [Schreuder, Frans](#) 
- [Kharraz, Oussama](#) 
-  Add maintainer

Partner team

Nikhef

✉ nikhef@opencores.org

README.md parser

Library of commonly used components :: Overview

Overview News Downloads Bugtracker

Edit pages Edit this page Help

Details

Name: common_components
Created: Oct 17, 2018
Updated: Oct 17, 2018
SVN Updated: Oct 18, 2018
SVN: [Browse](#)
Latest version: [download](#) (might take a bit to start...)
Statistics: [View](#)
[Bugs](#): 0 reported / 0 solved

★ Star 0 you like it: star it!

Other project properties EDIT

Category: [Library](#)
Language: [VHDL](#)
Development status: [Planning](#)
Additional info:
WishBone compliant: No
WishBone version: n/a
License: LGPL

☒ Use README.md from SVN repo

Description

Please write a description of the project here. It is used as a MetaTag (search engines looks at this).

Project maintainers

- [van der Schuur, Daniel](#)
- [Add maintainer](#)

Partner team

ASTRON
Netherlands Institute for Radio Astronomy
astron@opencores.org

What did we learn?

- Different labs have different needs, work-flows, processes, organization and cultures
- What is home-made might not be one-to-one ready for the general public
- Strive for simplicity and proper structure
- **Ponder about all the above makes the organization itself potentially better (our view)** → forces all of us to critically self assess

Plans for this year

- Better **indexing** and **searching** for the Cores
- Look into **GIT support**
- Improve overall interaction and **user experience** on the website
- Evaluate **design challenge** opportunities
- **Marketing** and **community management**

In the public domain



Europe's scientific community is helping to support a portal for access to free-to-use open-source cores with financial assistance for the OpenCores organization.

With the emergence of RISC-V in 2016 and 2017 open source hardware became a hot topic once again and a startup called Oliscience BV (Amsterdam, The Netherlands) was formed in 2017 to look after the OpenCores website and community. As a result, OpenCores, which was originally founded in 1999, is embarking on its third phase of ownership and is planning to emerge from a quiet period that lasted for several years.

In 2017, with support from Nikhef, the Dutch National Institute for Subatomic Physics, Andrea Borgia, a digital designer at the Nikhef electronics technology department, and colleagues, acquired ownership of the OpenCores website, control of the various files and formed Oliscience. The amount paid to previous owners for OpenCores has not been disclosed.

Oliscience is a contraction of open logic interconnects science, which reflects the company's origins in Europe's scientific community. The company's formation also reflects the fact that scientific researchers are frequent users of free IP cores and that they did not want to see OpenCores atrophy or disappear.

- Open Cores **rides again**
- Honoured in **OSDA** program

Workshop on Open Source Design Automation (OSDA) 2019

held in conjunction with the [Design, Automation and Test in Europe Conference \(DATE\)](#)
Friday, March 29, 2019; Florence, Italy

Final Programme

Registration Link

Note: Please select "Friday Workshop W10"

Gratefully acknowledge support from our sponsors:



In the public domain

- Mentioned in a report for the EU Commission...

EC publishes study on Next Generation
Internet 2025

NLnet and Gartner deliver study for EC's Next
Generation Internet initiative

[Deze tekst in het Nederlands 



Brussels/Amsterdam, October 5th 2018

<https://nlnet.nl/news/2018/20181005-NGI-Study-Report-en.html>

In the public domain

- Mentioned in a report for the European Commission (EC)...

EC publishes study on Next Generation Internet 2025



goals".

The European Commission's Directorate-General CNECT has published the much anticipated study "Next Generation Internet 2025", an in-depth analysis of the state of the internet performed by NLnet foundation and Gartner Europe. "We believe that the Next Generation Internet initiative has actual potential to vastly improve the internet and change the current course of the internet", states Michiel Leenaars, director of Strategy at NLnet and leader of the study. "The strategic topics we have identified in the report are essential to reach those

In the public domain

- ... and DARPA (US)



What about OpenCores?

Open Cores

- **1180 projects** (different IP-blocks)
- **283578 registered users**
- **1783 new registered users** during last month (August)
- **~500 000 page views** every month
- **~80 000 visitors** every month
- **~5:30 (min:sec)** Average time at website
- **~6 page views** per visitor (average)

Common Issues:

- Documentation
- Quality!
- Abandoned projects
- Lack of collaboration
- License Terms

Registered OpenCores users



283578

[OpenCores statistics](#)

Last updated projects

- [ODESS Multicore Project](#)
- [NoC based MPSoC](#)
- [PCIe Gen3x8 DMA for virtex7](#)
- [UART to Bus](#)
- [AUTO DATA-RATE CHECKER](#)
- [SpaceWireSystemC](#)
- [UART 16550 core](#)
- [MPEG2 Video decoder](#)

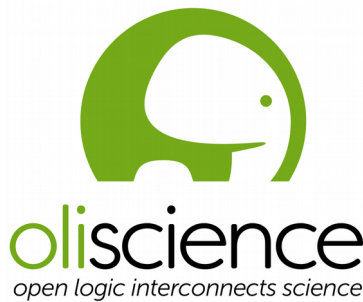
Most popular projects

- [USB Host Core](#)
- [I2C controller core](#)
- [NEO430 Processor \(MSP430-compatible\)](#)
- [SPI Master/Slave Interface](#)
- [Ethernet 10GE Low Latency MAC](#)
- [I2C master/slave Core](#)
- [Reed Solomon Decoder \(204,188\)](#)
- [SPI Verilog Master & Slave modules](#)

Distribution Statement "A" (Approved for Public Release, Distribution Unlimited)

https://www.darpa.mil/attachments/eri_design_proposers_day.pdf

Thank you



+



OpenCores

www.opencores.org

www.opencores.org

www.oliscience.nl

LinkedIn: <https://www.linkedin.com/company/oliscience/>

Twitter: @Oliscience101

CERN efforts

to share...
or...
to share more!

Javier Serrano from CERN

CERN efforts: sharing platform



HOME PROJECTS LICENSES COMPANIES

OPEN HARDWARE REPOSITORY

SIGN IN REGISTER

<http://www.ohwr.org>

PROJECTS



FEATURED PROJECTS

CERN BE-CO-HT contribution to KiCad

This project hosts documentation and code to be contributed by CERN's BE-CO-HT section to the KiCad PCB design tool.

[More info at the Wiki page](#)

CERN Open Hardware Licence

A project devoted to developing and discussing the CERN Open Hardware Licence.

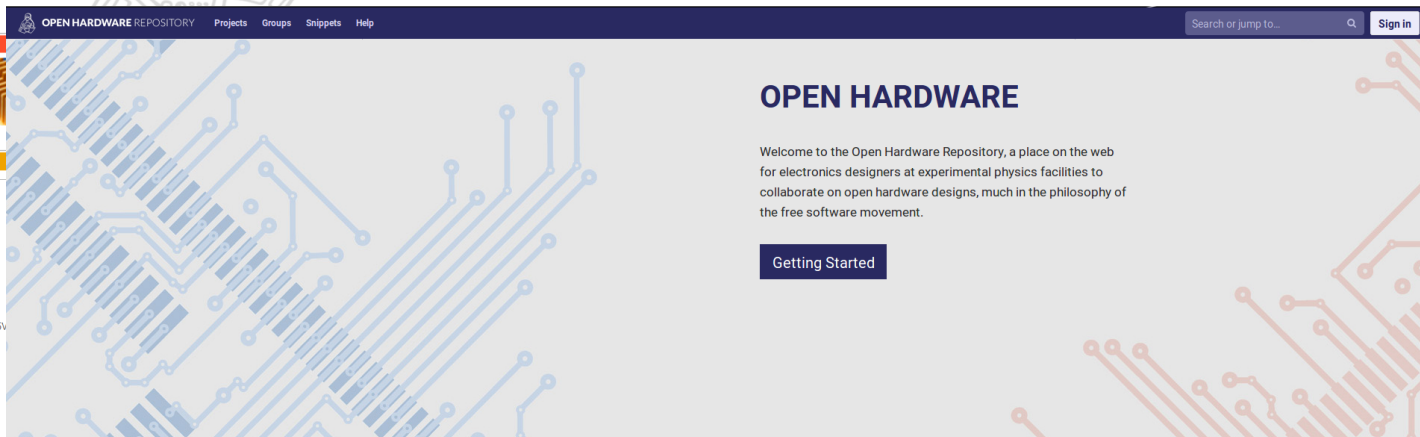
[More info at the Wiki page](#)

FMC ADC 100M 14b 4cha

FmcAdc100M14b4cha is a 4 channel 100MSPS 14 bit ADC low pin count FPGA Mezzanine Card (VITA 57). Input ranges: +/-50mV, +/-0.5V correction by +/- 5V is possible for each gain range. Commercially available.

[More info at the Wiki page](#)

FMC DEL 1ns 4cha



Projects

Licenses

Companies

Help

My account

Featured projects

CERN Open Hardware Licence

A project devoted to developing and discussing the CERN Open Hardware Licence. [More info at the Wiki page](#)

OHR Meta Project

A meta project used to discuss and present information about Open Hardware and related subjects. [More info at the Wiki page](#) [More info about the CERN Open Hardware licence](#) [More info about the OHR.org site support](#)

CERN BE-CO-HT contribution to KiCad

This project hosts documentation and code to be contributed by CERN's BE-CO-HT section to the KiCad PCB design tool. [More info at the Wiki page](#)

White Rabbit

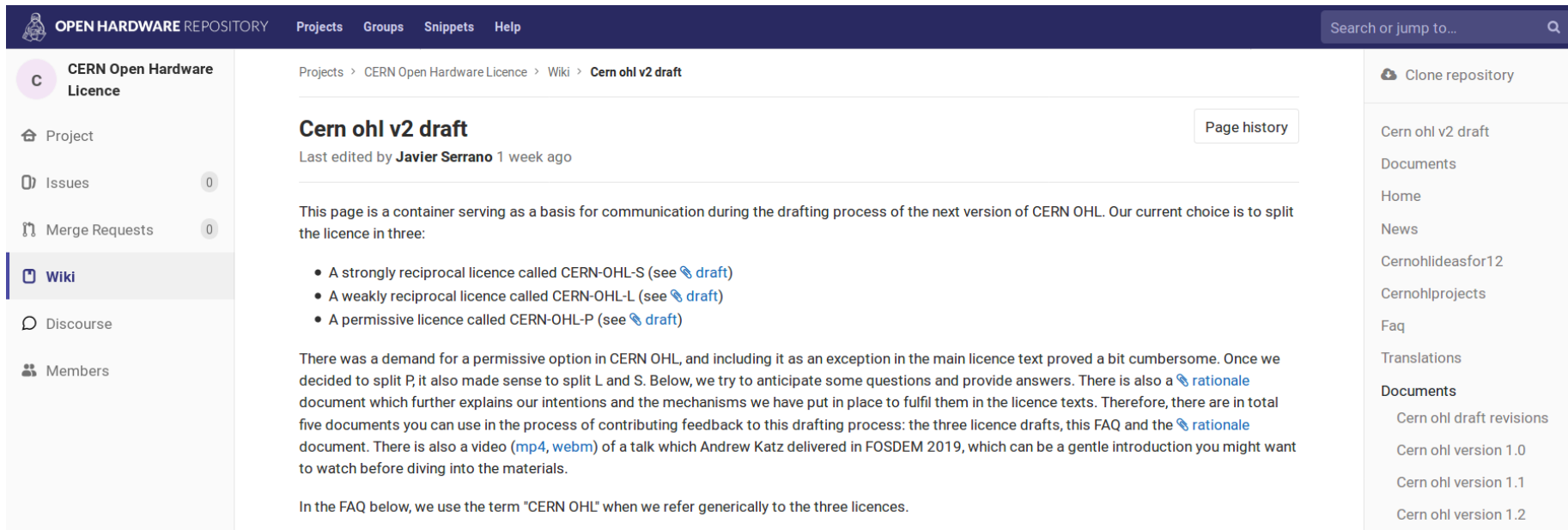
White Rabbit is a fully deterministic Ethernet-based network for general purpose data transfer and synchronization. It can synchronize over 1000 nodes with sub-ns accuracy over fiber lengths of up to 10 km. Commercially available. [More info at the Wiki page](#)

Simple PCIe FMC carrier SPEC

A simple 4-lane PCIe carrier for a low pin count FPGA Mezzanine Card (VITA 57). It supports the White Rabbit timing and control network. Commercially available. Linux and Labview drivers available for some mezzanine cards. [More info at the Wiki page](#)

- Migrated from Redmine to GitLab

CERN efforts: licensing



The screenshot shows the 'CERN Open Hardware Licence' page on the Open Hardware Repository. The page title is 'Cern ohl v2 draft', last edited by Javier Serrano 1 week ago. The content states: 'This page is a container serving as a basis for communication during the drafting process of the next version of CERN OHL. Our current choice is to split the licence in three:'. A bulleted list follows: '• A strongly reciprocal licence called CERN-OHL-S (see [draft](#))', '• A weakly reciprocal licence called CERN-OHL-L (see [draft](#))', and '• A permissive licence called CERN-OHL-P (see [draft](#))'. The text continues: 'There was a demand for a permissive option in CERN OHL, and including it as an exception in the main licence text proved a bit cumbersome. Once we decided to split P, it also made sense to split L and S. Below, we try to anticipate some questions and provide answers. There is also a [rationale](#) document which further explains our intentions and the mechanisms we have put in place to fulfil them in the licence texts. Therefore, there are in total five documents you can use in the process of contributing feedback to this drafting process: the three licence drafts, this FAQ and the [rationale](#) document. There is also a video ([mp4](#), [webm](#)) of a talk which Andrew Katz delivered in FOSDEM 2019, which can be a gentle introduction you might want to watch before diving into the materials.' It concludes with: 'In the FAQ below, we use the term "CERN OHL" when we refer generically to the three licences.'

<https://www.ohwr.org/projects/cernohl/wiki/cern-ohl-v2-draft>

- New draft version of the Open Hardware Licence (OHL) v2
- Better coverage for “gateware”